SECTION 6

INTERFACING TO ADCs AND DACs

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SECTION 6

INTERFACING TO ADCs AND DACs

Walt Kester

This section examines the fundamentals of interfacing to ADCs and DACs. ADC inputs require an appropriate drive amplifier to buffer the signal and provide gain and offset capability. DAC outputs may also require buffering. Both ADCs and DACs require low-jitter sampling clocks to control the conversion rate, some require external voltage references, and all require proper attention to layout, signal routing, power supply generation and decoupling, and grounding.

ADC AND DAC INTERFACING

- ADC Input / DAC Output Amplifier
- External Reference Voltage Generation
- Capturing ADC Output Data / Buffering DAC Input Data
- Sampling Clock Generation
- Proper Layout and Signal Routing
- Power Supply Generation, Filtering, Decoupling
- Proper use of Ground Planes and Grounding Techniques

Figure 6.1

DRIVING ADC INPUTS

Selecting the appropriate drive amplifier for an ADC involves many considerations. Because the ADC drive amplifier is in the signal path, its error sources (both dc and ac) must be considered in calculating the total error budget. Ideally, the ac and dc performance of the amplifier should be such that there is no degradation of the ADC performance. It is rarely possible to achieve this, however; and therefore the effects of each amplifier error source on system performance should be evaluated individually.

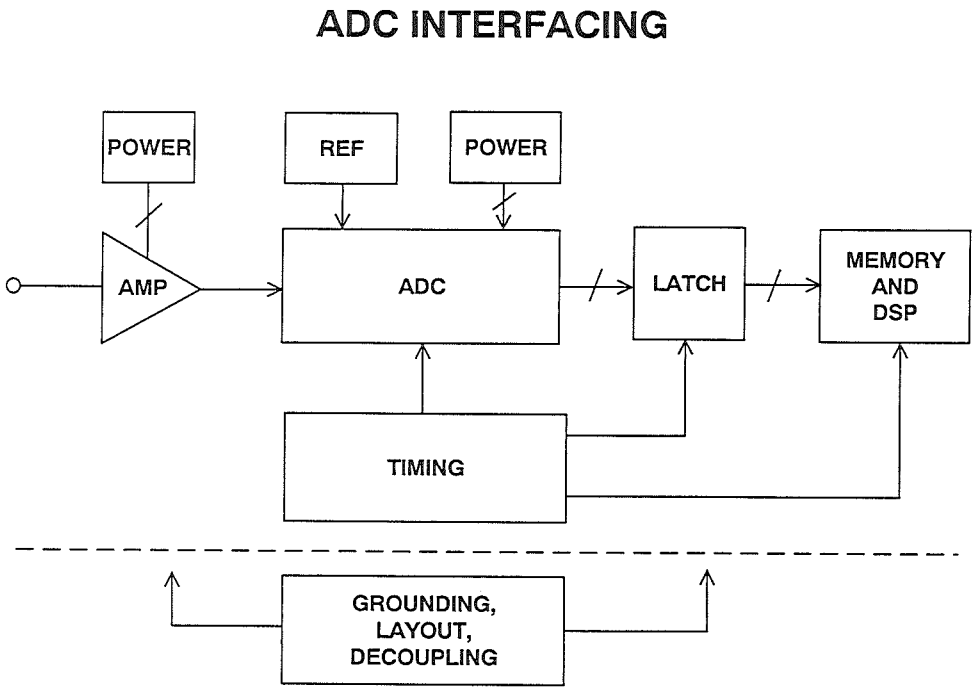


Figure 6.2

Evaluating and selecting op-amps based on the dc requirements of the system is a relatively straightforward matter. For many applications, however, it is more desirable first to select an amplifier on the basis of ac performance (bandwidth, THD, Noise, etc.) The ac characteristics of ADCs are specified in terms of SNR, ENOBs, and distortion. The drive amplifier should have performance which is better than that of the ADC so that maximum dynamic performance is obtained (see Figure 6.4.). If the amplifier ac performance is adequate, the dc specifications should then be examined in terms of system performance.

ADC DRIVE AMPLIFIER CONSIDERATIONS

- AC Performance -
  - Bandwidth, Settling Time
  - Harmonic Distortion, Total Harmonic Distortion
  - Noise, THD + Noise
- DC Performance -
  - Gain, Offset, Drift
  - Gain Non-Linearity
- As a general principle, select first for AC performance, then evaluate DC performance.
- Always consult the data sheet for recommendations!!

Figure 6.3

THE DISTORTION AND NOISE PERFORMANCE OF THE DRIVE AMPLIFIER SHOULD BE BETTER THAN THE ADC

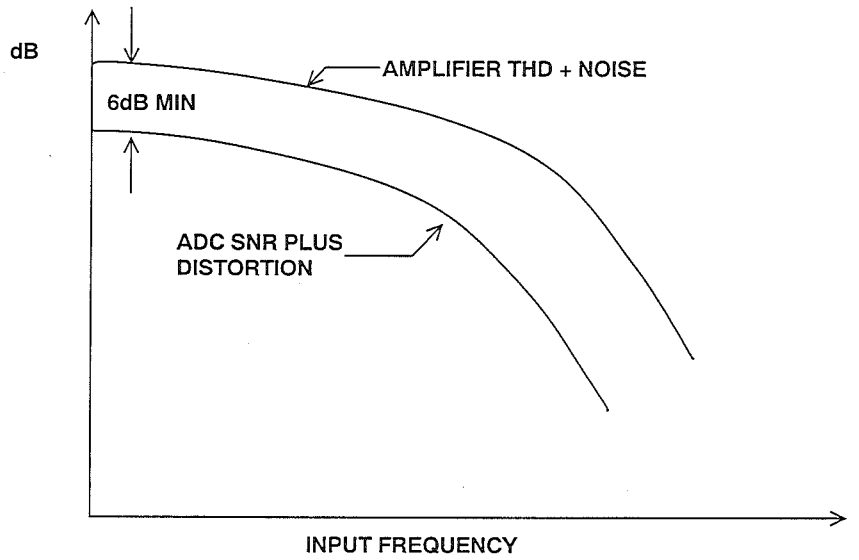


Figure 6.4

One must also understand the analog input circuit of the ADC and its effect on the amplifier. Flash converters generally present a varying capacitive load to the amplifier which may cause instability and distortion. Sampling ADCs often present rather benign loads to the drive amplifier because of their internal track-and-hold. However, some sampling ADC architectures, such as switched-capacitor or sigma-delta, may generate current spikes from which the drive amplifer must quickly settle. A simple model for estimating transient settling time is shown in Figure 6.5. The closed-loop output impedance of an op-amp increases with frequency and may be as great as several hundred ohms at high frequencies due to the equivalent output inductance of the complementary emitter follower output stage. The transient load current will develop a transient voltage across this impedance at the op amp output. This small perturbation will decay exponentially with a time constant equal to $1/2\pi f_{cl}$ (f_{cl}= closed loop bandwidth) if the op-amp exhibits single pole response. The simple exponential decay formula can be used to determine the settling to any desired accuracy.

SMALL SIGNAL MODEL ALLOWS ESTIMATION OF OP AMP SETTLING TIME DUE TO TRANSIENT LOAD CURRENT

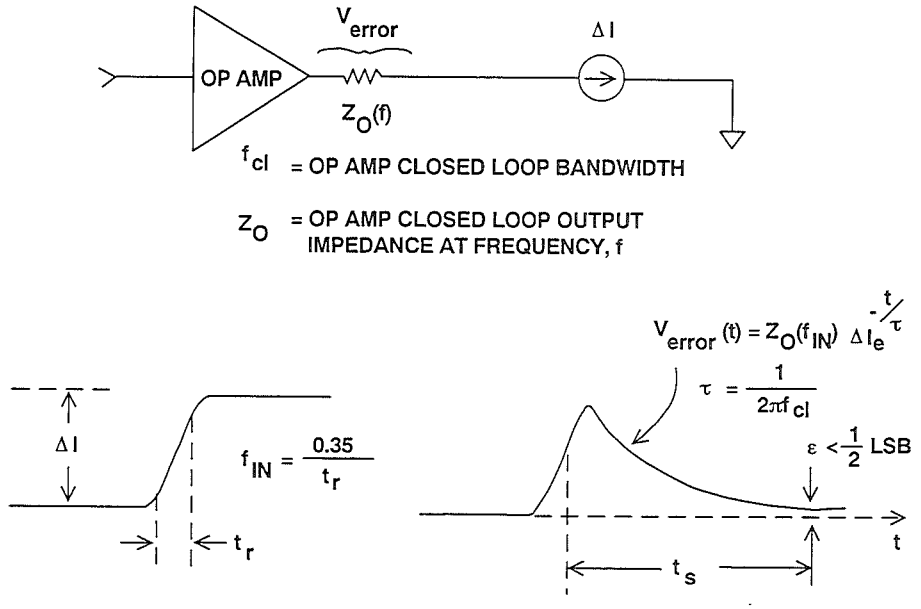


Figure 6.5

Settling from transient load currents is not generally a problem in an op-amp which has been properly selected to drive sampling converters. The op-amp small-signal bandwidth will generally be high (with respect to the sampling rate) in order to achieve low levels of distortion. The wide bandwidth will automatically yield fast settling to transient currents if they are present.

While it is important to understand the concepts presented above regarding op-amp selection, ADC manufacturers such as Analog Devices generally recommend appropriate drive amplifiers in their data sheets, so the selection process is relatively straightforward in most cases.

ADC INPUT CLAMPING AND PROTECTION CIRCUITS

Most ADCs will tolerate out-of-range signals in the order of 50% or so without damage to the input circuit, provided the overvoltage does not go outside the supplies. An exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of ±5V should tolerate an input signal up to ±7.5V. The overvoltage recovery time of an ADC (Figure 6.6) usually increases as the input signal moves further out of range.

ADC OVERVOLTAGE RECOVERY TIME

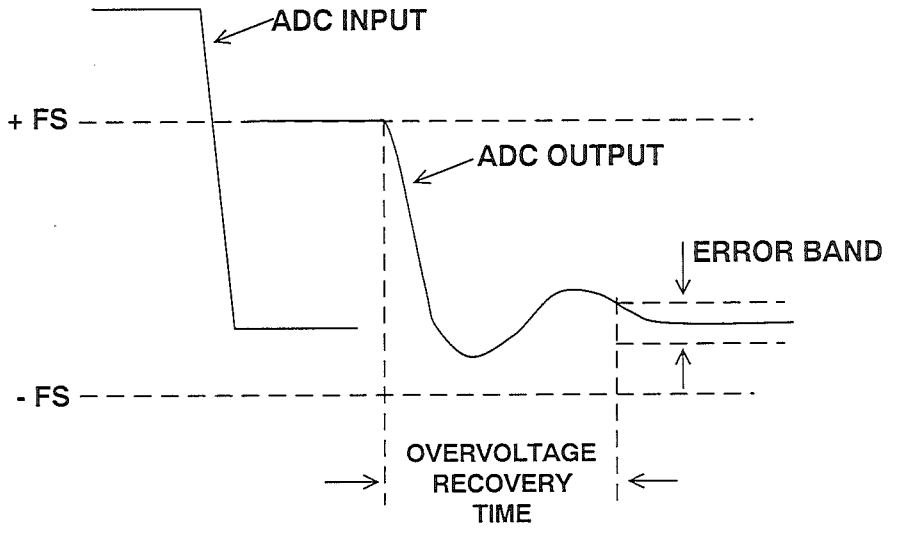


Figure 6.6

It may therefore be desirable to clamp the ADC input so that the input signal is limited to small overrange values, especially if large out-of-range signals are frequent. Clamping not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time. Because the clamping circuit is in the signal path, care must be taken to insure that it does not degrade the system performance for normal signals. Specially designed low distortion amplifiers, such as the AD8036 and AD8037, contain internal clamping circuits and are ideal for this purpose. Recovery time from overdrive is less than 5ns.

Other conditions of temporary overvoltage may occur because of power supply sequencing. Several possibilities will be discussed briefly.

Figure 6.7 shows an op amp powered by ±15V supplies driving an ADC which is powered by ±5V supplies (typical of many CMOS ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, many CMOS ADCs have the protection diodes on-chip.

PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO POWER SUPPLY SEQUENCING

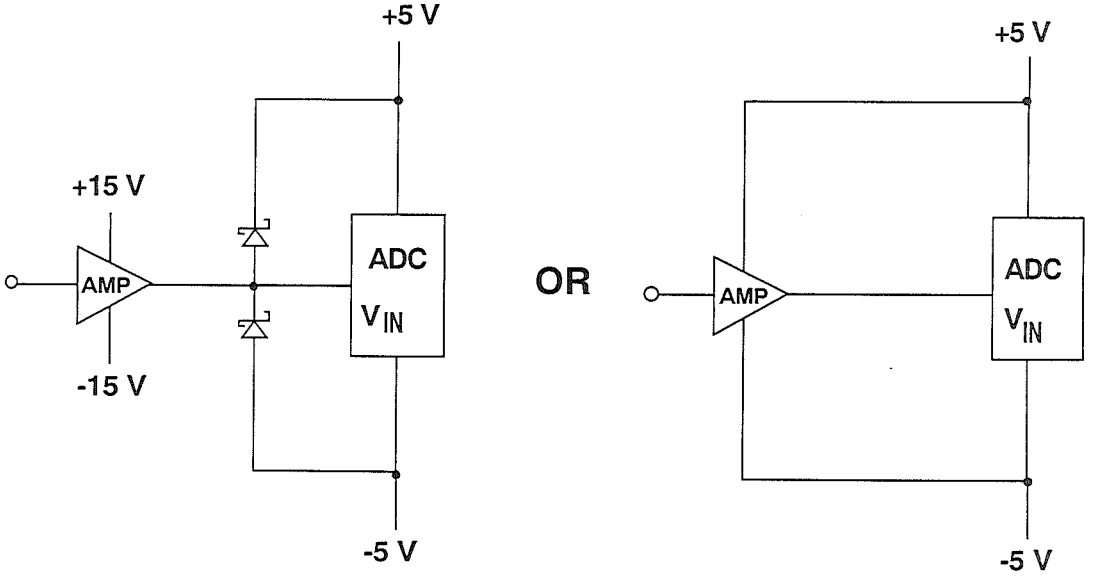


Figure 6.7

An alternative is also shown in Figure 6.7. If a ±5V supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both ±15V and ±5V supply operation. If a ±15V op amp must be used, the ±5V for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 6.8. This is relatively efficient because most CMOS ADCs are low power devices, and is preferable to powering a ±5V CMOS converter from noisy ±5V logic supplies.

USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

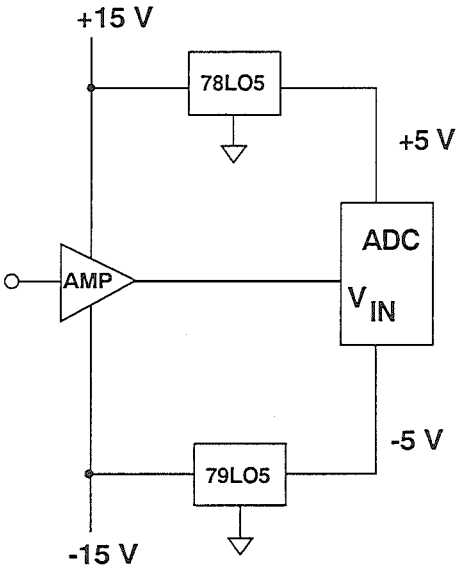


Figure 6.8

Many flash converters are designed to operate on a single –5.2V power supply and have a negative input voltage range of 0 to –2V. If the input goes positive, the substrate silicon diode begins to conduct. Forward current above a few mA may permanently degrade the performance of the flash converter. Input Schottky diodes should be installed as shown in Figure 6.9 to prevent this happening. Most amplifiers suitable for driving flash converters operate on dual 5V supplies and can deliver 50 to 100mA of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than 50mA current is expected from the drive amplifier.

PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

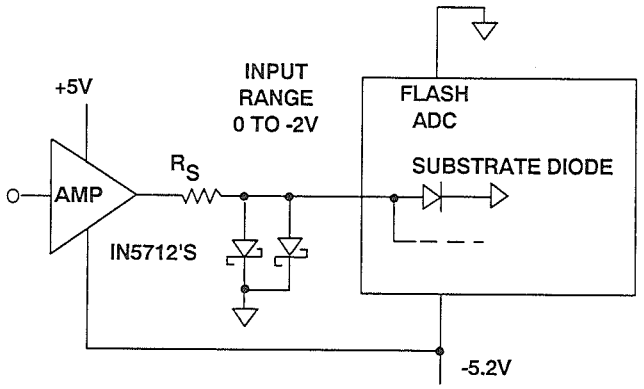


Figure 6.9

EFFECTIVE INPUT NOISE OF ADCS

Wide bandwidth 12 to 16-bit sampling ADCs behave differently from non-sampling 12-bit SAR ADCs such as the AD574. Ideally, a fixed dc input to an ADC should result in the same output code for each conversion (of course, the dc input should be centered between the transition regions of the two adjacent codes). In the past, ADCs were analyzed for code transition noise using a DAC to reconstruct the analog signal. A very slow ramp voltage was applied to the ADC, so that each code transition could be observed. In a high-resolution sampling converter, for a given input voltage, a range of output codes may occur. This is because of unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to a precision sampling ADC (such as the 16-bit, 166kSPS AD7884/AD7885) and several thousand outputs are recorded, a distribution of codes such as that shown in Figure 6.10 will result.

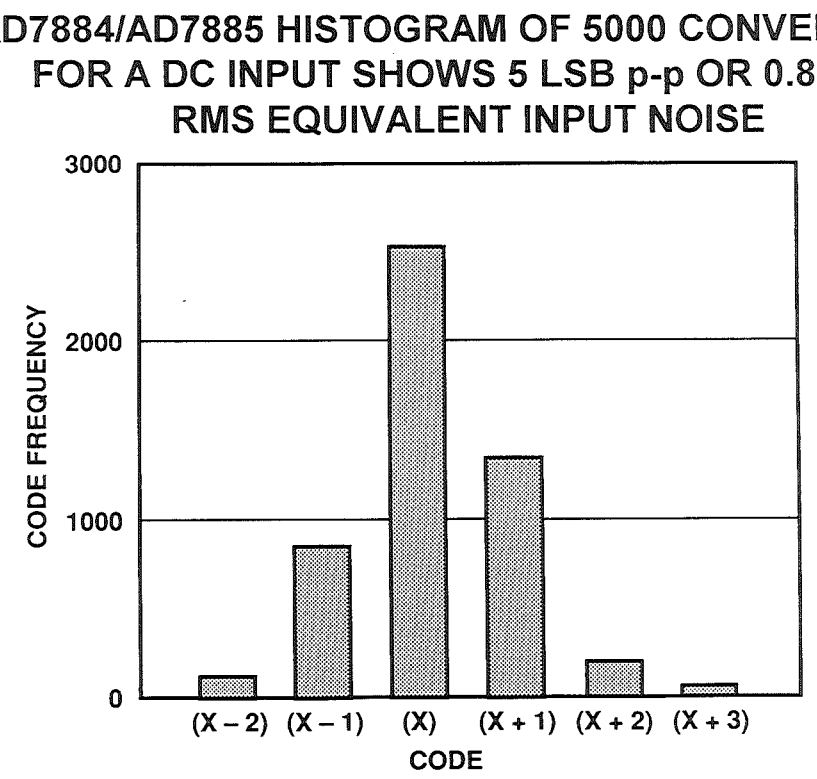


Figure 6.10

The correct code appears most of the time, but adjacent codes appear as well with reduced probability. If a Gaussian probability distribution is fitted to the histogram, the standard deviation is approximately equivalent to the equivalent input rms noise of the ADC. The actual specification on the ADC data sheet may be given in terms of a histogram or may be converted into an equivalent input rms noise voltage. In Figure 6.10, the peak-to-peak noise is about 5 LSBs, corresponding to 5/6 = 0.8 LSBs rms (Peak-to-peak values may be converted into rms values by dividing by 6). For a 6V input span, this corresponds to 74μV rms equivalent input noise.

This noise may come from several sources. For example, a 1MΩ resistor generates 158μV rms noise over a 1MHz single-pole bandwidth (the equivalent noise bandwidth is 1.57MHz). One LSB for the AD7884 operating with a 6V peak-to-peak input range is 92μV. This illustrates the importance of keeping the source impedances low. Some of the internal ADC noise is generated in the wideband SHA. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD7884/AD7885 has an input bandwidth which exceeds 1MHz, even though the maximum sampling rate is 166kSPS). These wide bandwidth front ends are required in order to minimize gain and phase distortion at the signal frequencies and to optimize performance in undersampling applications. A certain amount of unavoidable noise is generated in the SHA and the other wideband circuits within the ADC which cause the sample-to-sample variation in output codes for dc inputs. Good layout, grounding, and decoupling techniques are essential to prevent additional external noise from coupling into the ADC and adding to the inherent equivalent input noise.

DRIVE AMPLIFIER NOISE CONSIDERATIONS

Most sampling ADCs have input bandwidths much greater than their maximum sampling rate f_S. The ADC drive amplifier must also have wide bandwidth, generally greater than the ADC. Any output noise generated by the op-amp must therefore be integrated over the full input bandwidth of the ADC as shown in Figure 6.11. This rms noise should be calculated and compared with the ADC input noise specification. Details of how to perform this calculation are given in Section 1.The op-amp output noise should be 2 to 3 times less than the ADC input noise. If this is not the case, a lower-noise op-amp should be selected.

If the input-referred noise of the ADC is not specified, then the op-amp output noise should be compared to the theoretical quantization noise, $q/\sqrt{12}$. Again, it should be 2 to 3 times less.

The effects of op-amp noise are reduced by placing the anti-aliasing filter between the amplifier and the ADC input. The op-amp noise is then only integrated over the bandwidth of the anti-aliasing filter. In undersampling applications, the anti-aliasing filter will be a *bandpass* rather than an *lowpass* filter.

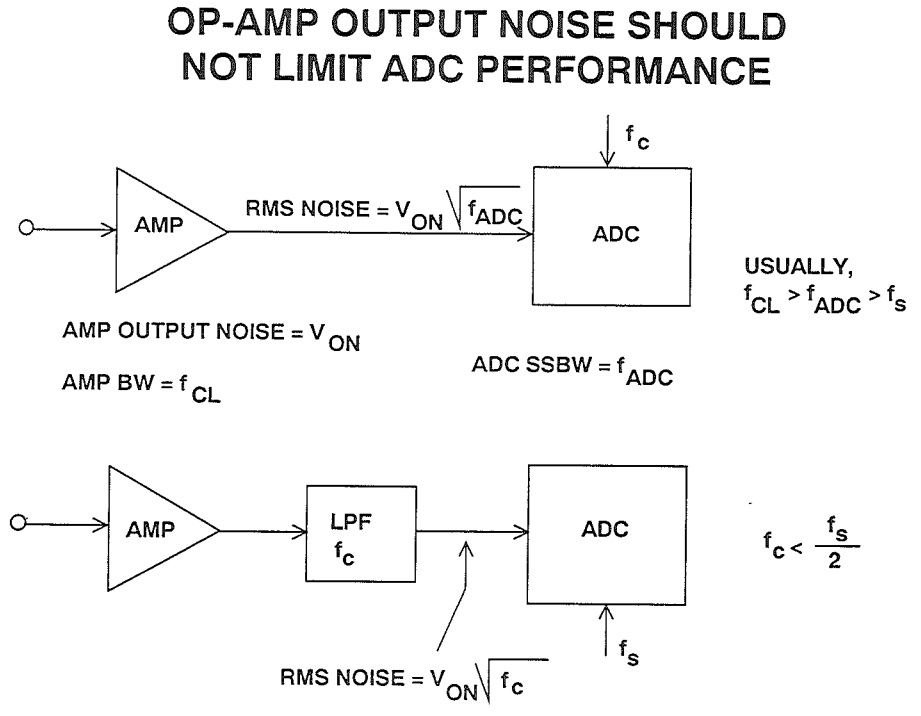


Figure 6.11

ADC REFERENCE VOLTAGE CONSIDERATIONS

Many ADCs have internal voltage references, others do not. If the ADC has an internal reference, it is often pinned-out so that an external reference can be used to provide better stability and lower noise. External references generally perform better than internal ones because the IC processes used for data converters are less than ideal for precision low-noise references. Sometimes, however, the internal reference is not very accurate, but the ADC is trimmed to high accuracy using whatever reference voltage the internal reference supplies. In such cases, an accurate external reference voltage may actually reduce the converter's dc accuracy.

INTERNAL VERSUS EXTERNAL DATA CONVERTER REFERENCES

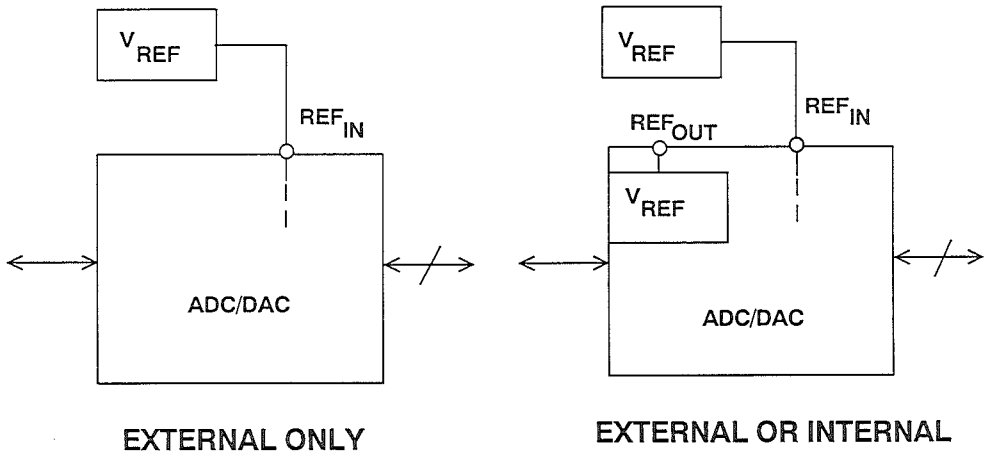


Figure 6.12

The reference voltage is important because it establishes the fullscale range of the ADC, and the overall dc accuracy and stability of the ADC can be no better than that of the reference. Standard monolithic reference voltages are 2.5V, 3V, 5V, and 10V. Noise on the ADC reference generally translates directly into increased internal noise levels and degraded SNR performance.

The entire voltage reference function is available in ICs which utilize laser trimmed thin film resistors for excellent accuracy and low drift. Standard dc specifications for such a voltage reference are output current capability, line regulation, load regulation, output voltage tolerance, and output voltage change with temperature. AC specifications include turn-on settling time,

transient load current settling time, and noise. Selecting voltage references based on dc requirements is relatively straightforward. Evaluating its noise performance deserves further discussion.

Most voltage references specify peak-to-peak noise in a 0.1Hz to 10Hz bandwidth. For instance, the AD586 (a 5V buried zener reference with on-chip output buffer) specification in this bandwidth is 4μV peak-to-peak. In most sampling ADC applications, however, the wideband noise is usually of more concern. For the AD586, the unfiltered noise in a 1MHz bandwidth is approximately 200μV peak-to-peak, corresponding to 200/6 = 33μV rms. This value is usually larger for bandgap voltage references such as the REF-02 (800μV peak-to-peak). Regardless of the type of reference chosen, proper external filtering can virtually eliminate the wideband noise.

Some voltage references, such as the AD586, have a pin brought out designated as the noise reduction pin (see Figure 6.13). Connecting an external capacitor between ground and this pin forms a single-pole lowpass filter with an internal 4000Ω resistor. For instance, an external 1μF capacitor produces a single-pole corner frequency of approximately 40Hz. This filter virtually eliminates the broadband buried-zener noise, but the output buffer amplifier (approximate bandwidth is 1MHz) still produces approximately 160μV peak-to-peak noise in the 1MHz bandwidth, so the capacitor is not as useful as might be expected. It also greatly increases the reference startup time.

PRECISION LOW NOISE ADC VOLTAGE REFERENCE

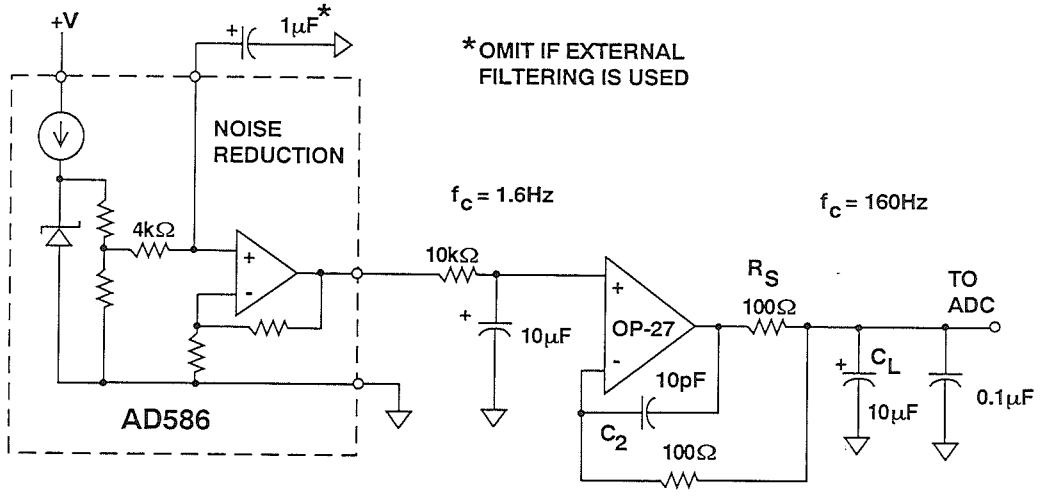


Figure 6.13

If low noise is required, adding a large capacitor on the reference output (10μF) will reduce the noise somewhat. This, however, may not produce the expected results for two reasons. First, the voltage reference output buffer amplifier has a low closed-loop output impedance, on the order of a few ohms at low frequencies. The additional large capacitor does little to reduce this impedance further. Second, loading the output of the internal op amp with a large capacitor may cause the op amp to become unstable and to oscillate or ring under transient load conditions. (This is not the case with the AD780 2.5V/3V reference which is designed to be stable regardless of its capacitive load).

The ideal solution in precision applications is to use an external filter such as the one shown in Figure 6.14. The 10kΩ resistor and the 10μF capacitor form a single-pole passive filter which has a corner frequency of 1.6Hz, and reduces the noise to approximately the value specified in the 0.1 to 10Hz frequency band (4μV peak-to-peak for the AD586 and the AD780). This passive filter is followed by a precision low noise buffer amp such as the OP-27 (V_n= 3nV/√Hz). The large load capacitor C_L = 10μF) serves two purposes. First, it forms a lowpass filter with R_S having a corner frequency of approximately 160Hz. This reduces the output voltage noise of the op amp to a negligible value. Second, it provides additional reference voltage stability by acting as a charge reservoir to any transient load current. This amount of capacitance is a heavy load on any op amp; therefore, R_S and C_2 compensate for the pole introduced by C_L and the op amp's output resistance. This compensation scheme ensures that the buffer circuit recovers and settles from the output transients quickly without the long settling tails that might produce conversion errors. The 0.1μF capacitor in parallel with C_L is to keep the output impedance low at high frequencies, where the large 10μF electrolytic capacitor becomes less effective.

When using external filtering, do not decouple the noise reduction pin of the reference (if it has one) with a capacitor as it will increase the reference startup time.

In applications where filtering the voltage reference noise is not required, the decoupling capacitors on the ADC reference voltage input terminal may be eliminated completely. Simply buffer the voltage reference output with a precision low noise high bandwidth amplifier which has sufficient transient load settling time, such as the AD845 (see Figure 6.14). This approach will minimize the need for additional components, but dc precision and noise performance will be sacrificed.

WIDEBAND LOW-NOISE BUFFER AMPLIFIER ELIMINATES THE NEED FOR LARGE DECOUPLING CAPACITORS

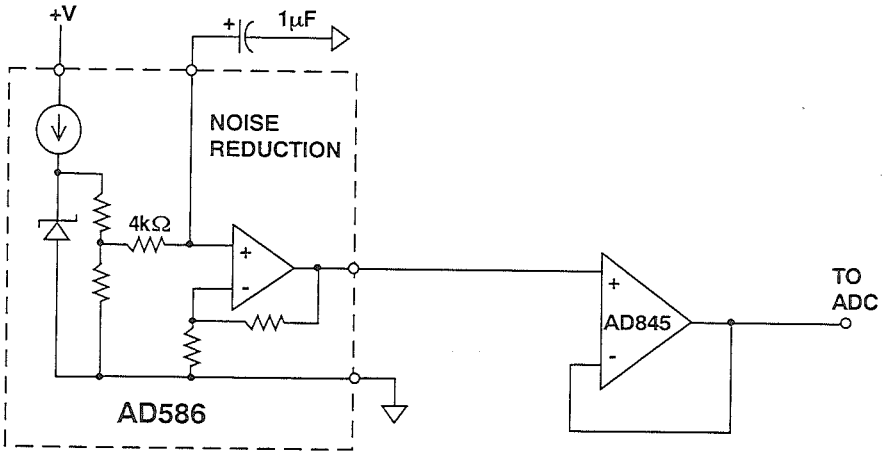


Figure 6.14

CAPTURING ADC OUTPUT DATA

There are basically two output formats for ADC data: parallel and serial. We will deal first with the parallel case. Flash converters are parallel output devices. A typical timing diagram for a flash converter (AD9048 8-bit, 35MSPS ADC) is shown in Figure 6.15. The conversion process is initiated by the rising edge of the CONVERT pulse. The output data begins to change toh ns later and settles tpd ns after the rising edge. The data is then valid and may be clocked into an external register. Notice, however, that the data corresponds to the sample taken by the previous convert pulse, i.e., there is a one-clock-cycle *pipeline* delay. This is typical in flash converters because of an internal latch as shown in the AD9048 block diagram (Figure 6.16). The clock to the external latch should be positioned somewhere within the interval in which the output data is stable. In many cases the leading or trailing edge of the CONVERT signal can be used for this purpose. The data sheet for the particular device should be consulted for specific timing details. It is highly recommended that a buffer latch be used between the ADC and the memory or data bus. The reasons will be discussed in more detail later in this section.

AD9048 8-BIT, 35MSPS FLASH CONVERTER TIMING DIAGRAM SHOWS PIPELINE (LATENCY) DELAY IN THE OUTPUT DATA

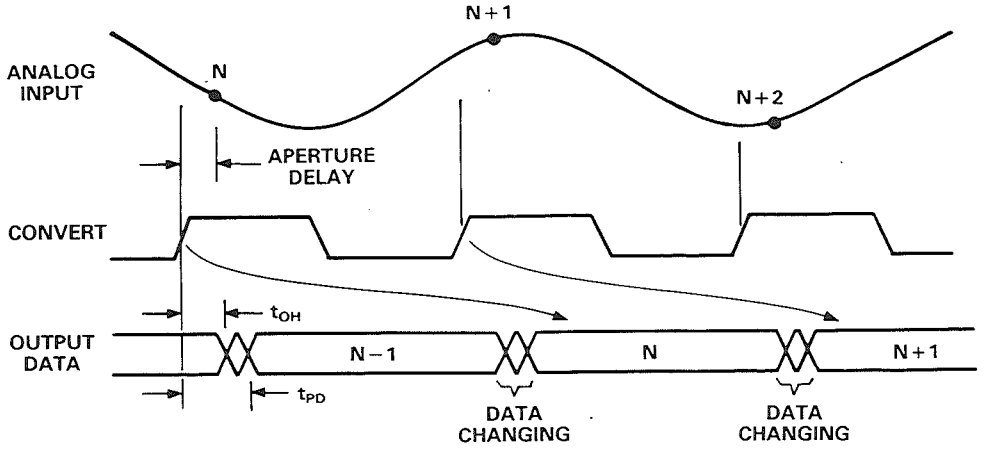


Figure 6.15

6

BLOCK DIAGRAM OF THE AD9048 FLASH CONVERTER

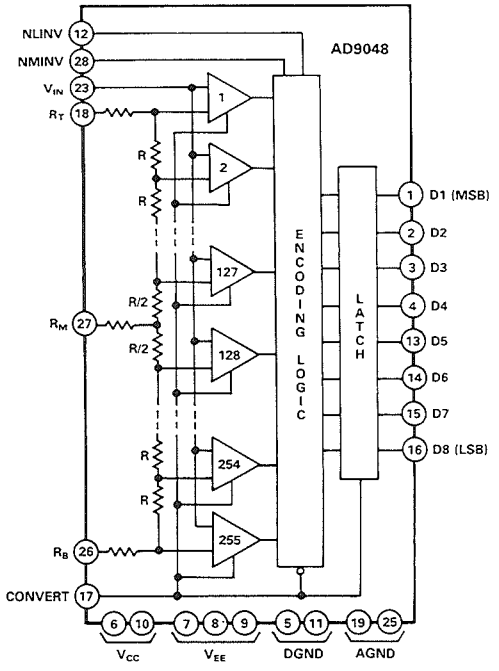


Figure 6.16

Subranging ADCs may have several clock cycles of pipeline delay, or latency. A block diagram of the AD872 12-bit, 10MSPS ADC is shown in Figure 6.17. The conversion is implemented using a 4-stage pipelined multiple flash architecture with error correction. The timing diagram for the device is shown in Figure 6.18. Note that there are three clock-cycle delays in the output data.

AD872 12-BIT, 10MSPS PIPELINED ADC ARCHITECTURE

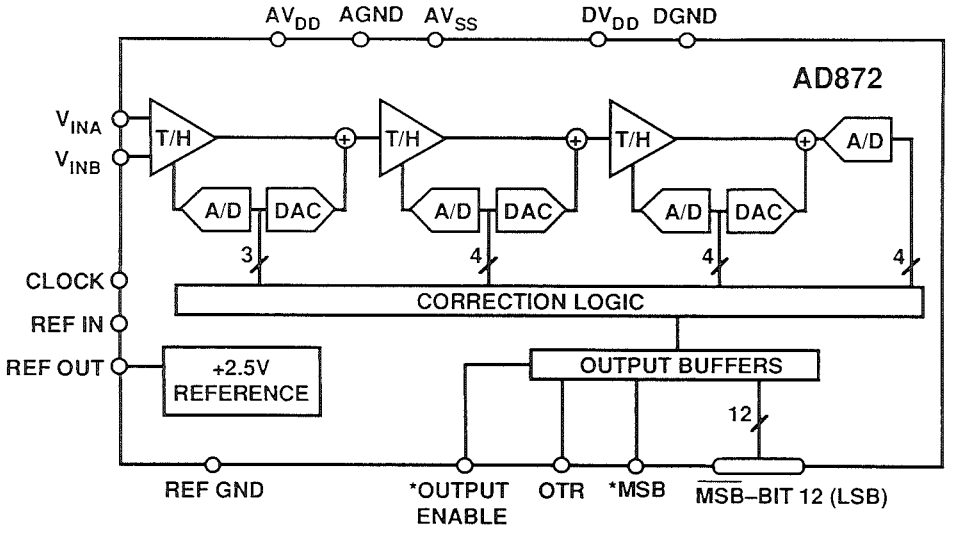


Figure 6.17

In most high speed applications, the output data from the ADC must be downloaded into a buffer memory for further processing. In order to avoid costly high speed, high power memory, the demultiplexing scheme shown in Figure 6.19 may be used to reduce the data output rate. This will allow low cost CMOS memory to be used for storage of the bulk of the data. High speed flash converters may provide on-chip demultiplexing to ease the demands on the buffer memory interface.

AD872 TIMING DIAGRAM SHOWS 3 CLOCK-CYCLE LATENCY

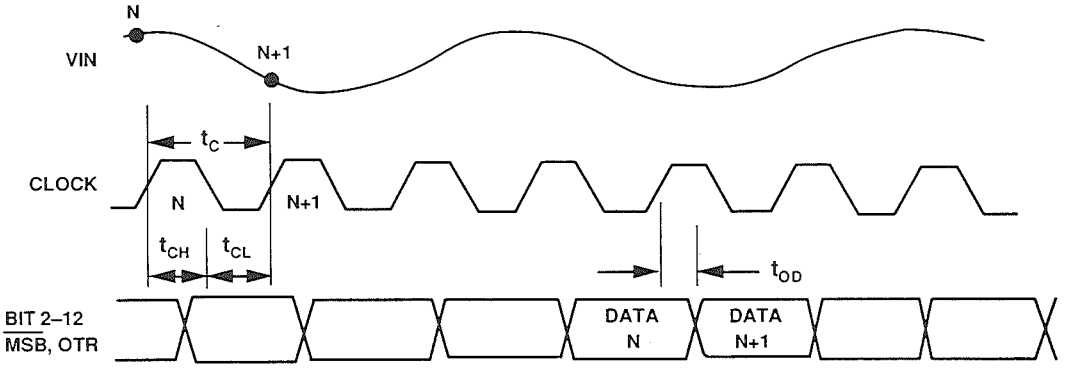


Figure 6.18

DEMULTIPLEXING HIGH SPEED ADC OUTPUTS FOR STORAGE IN SLOWER MEMORIES

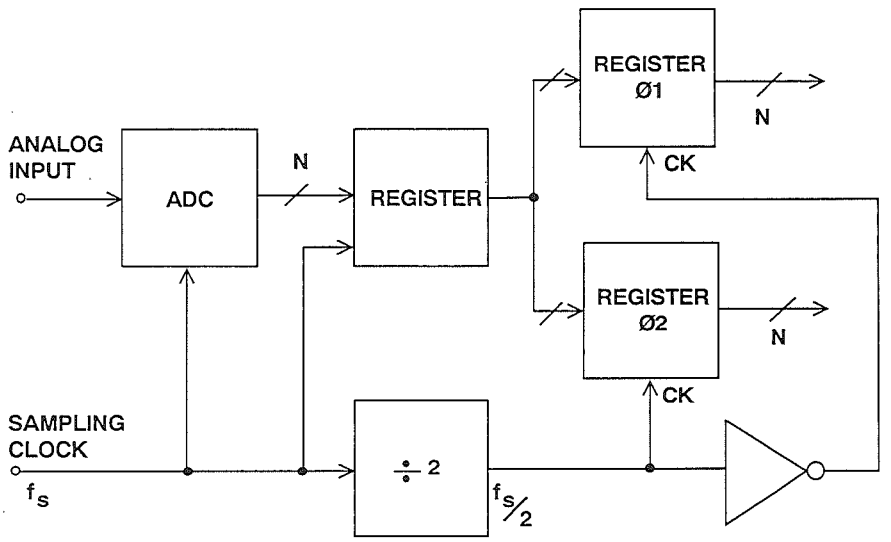


Figure 6.19

INTERFACING ADC OUTPUTS TO DSPS IN REALTIME SIGNAL PROCESSING APPLICATIONS

Realtime DSP processing of ADC data has become widespread because of faster ADCs and DSPs. The precision sampling ADCs used in these applications will have either parallel data outputs (one pin per bit), or a single serial output data line. The parallel case will be considered first.

Many parallel output sampling ADCs offer three-state outputs which can be enabled or disabled using an *output enable* pin on the IC. While it may be tempting to connect these three-state outputs directly to a backplane data bus, severe performance-degrading noise problems will result. All ADCs have a small amount of internal stray capacitance between the digital outputs and the analog input (typically 0.1 to 0.5pF). Every attempt is made during the design and layout of the ADC to keep this capacitance to a minimum. However, if there is excessive overshoot and ringing and possibly other high frequency noise on the digital output lines (as would probably be the case if the digital outputs were connected directly to a backplane bus) this digital noise will couple back into the analog input through the stray capacitance. The effect of this noise is to decrease the overall ADC SNR and ENOB. Any code-dependent noise will also tend to increase the ADC harmonic distortion.

The best approach to eliminating this potential problem is to provide an intermediate three-state output buffer latch which is located close to the ADC data outputs. This latch serves to isolate the noisy signals on the data bus from the ADC data outputs, thereby minimizing any coupling back into the ADC analog input.

The ADC data sheet should be consulted regarding exactly how the ADC data should be clocked into the buffer latch. Usually, a signal called *conversion complete*, or *busy* is provided from the ADC for this purpose.

It is also a good idea not to access the data in the intermediate latch during the actual conversion time of the ADC. This practice will further reduce the possibility of corrupting the ADC analog input with noise. The manufacturer's data sheet timing information should indicate the most desirable time to access the output data.

Figure 6.20 shows a simplified parallel interface between the AD676 16 bit, 100kSPS ADC (or theAD7884) and the ADSP-2101 microcomputer. (Note: the actual device pins shown have been relabled to simplify the following general discussion). In a realtime DSP application (such as in digital filtering) the processor must complete its series of instructions within the ADC sampling interval. Note that the entire cycle is initiated by the sampling clock edge from the sampling clock generator. Even though some DSP chips offer the capability to generate lower frequency clocks from the DSP master clock, the use of these signals as precision sampling clock sources is not recommended due to the probability of timing jitter. It is preferable to generate the ADC sampling clock from a well-designed low noise crystal oscillator circuit as has been previously described.

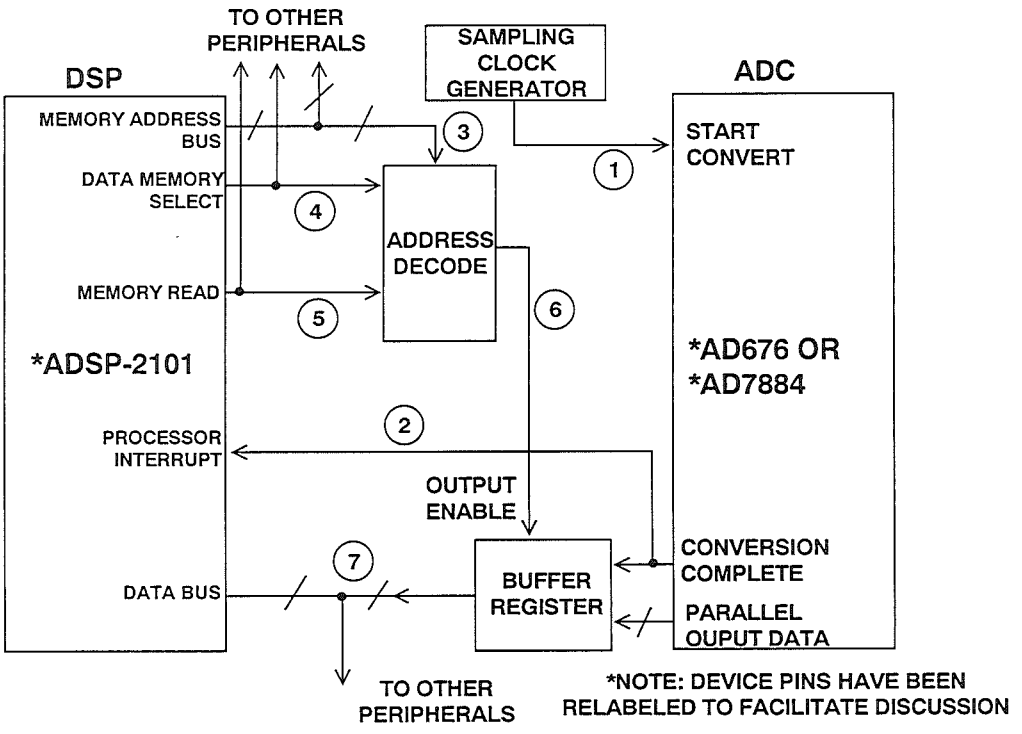


Figure 6.20

The sampling clock edge initiates the ADC conversion cycle. After the conversion is completed, the ADC *conversion complete* line is asserted which in turn interrupts the DSP. The DSP then places the address of the ADC which generated the interrupt on the *data memory address* bus and asserts the *data memory select* line. The *read* line of the DSP is then asserted. This enables the external three-state ADC buffer register outputs and places the ADC data on the *data bus*. The trailing edge of the *read* pulse latches the ADC data on the *data bus* into the DSP internal registers. At this time, the DSP is free to address other peripherals which may share the common data bus.

Because of the high-speed internal DSP clock (50MHz for the ADSP-2101), the width of the *read* pulse may be too narrow to access properly the data in the buffer latch. If this is the case, adding the appropriate number of programmable software wait states in the DSP will both increase the width of the *read* pulse and also cause the *data memory select* and the *data memory address* lines to remain asserted for a correspondingly longer period of time. In the case of the ADSP-2101, one wait state is one instruction cycle, or 80ns.

ADCs which have a serial output (such as the AD677, AD776, and AD1879) are interfaced to the serial port of many DSP chips as shown in Figure 6.21. The sampling clock is generated from the low-noise oscillator. The ADC output data is presented on the *serial data* line one bit at a time. The *serial clock* signal from the ADC is used to latch the individual bits into the serial input shift register of the DSP serial port. After all the serial data is transferred into the

serial input register, the serial port logic generates the required processor interrupt signal. The advantages of using serial output ADCs are the reduction in the number of interface connnections as well as reduced noise because there are fewer noisy digital PC tracks close to the converter. In addition, SAR and Sigma-Delta ADCs are inherently serial-output devices. The number of peripheral serial devices permitted is limited by the number of serial ports available on the DSP chip.

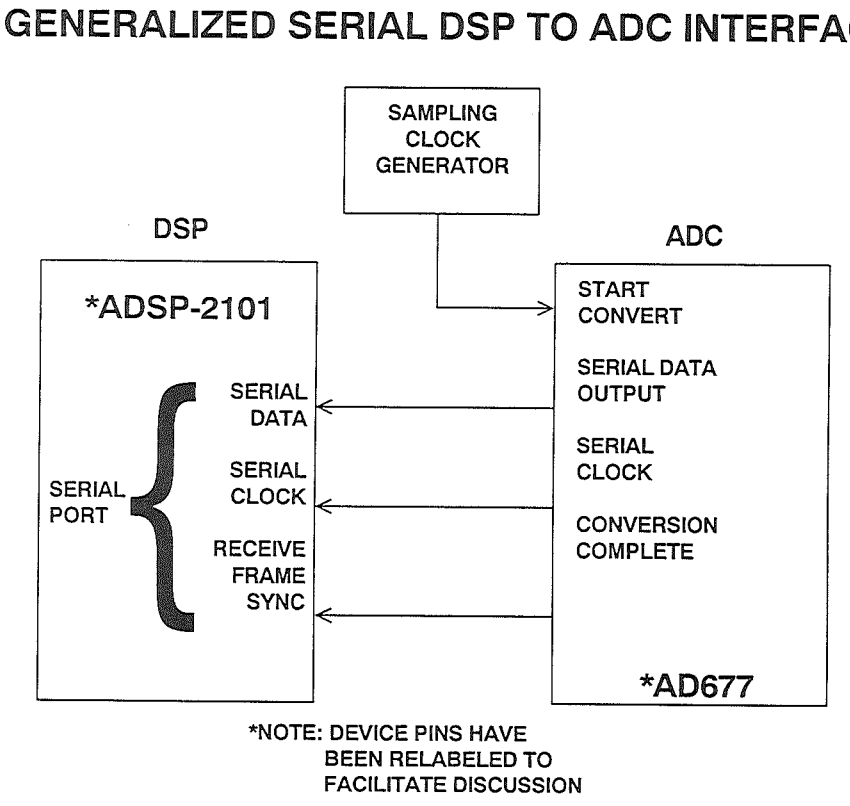


Figure 6.21

INTERFACING TO DACS

Most of the principles previously discussed regarding interfacing to ADCs also apply to DACs. A generalized block diagram of a parallel input DAC is shown in Figure 6.22. Most high performance DACs have an internal parallel DAC Latch which drives the actual switches. This latch deskews the data so that the output glitch is minimized. Some DACs designed for realtime sampled-data DSP applications have an additional input latch so that the input data can be loaded asynchronously with respect to the DAC Latch Strobe. Some DACs have an internal reference voltage which can either be used or bypassed with a better external reference. Other DACs require an external reference.

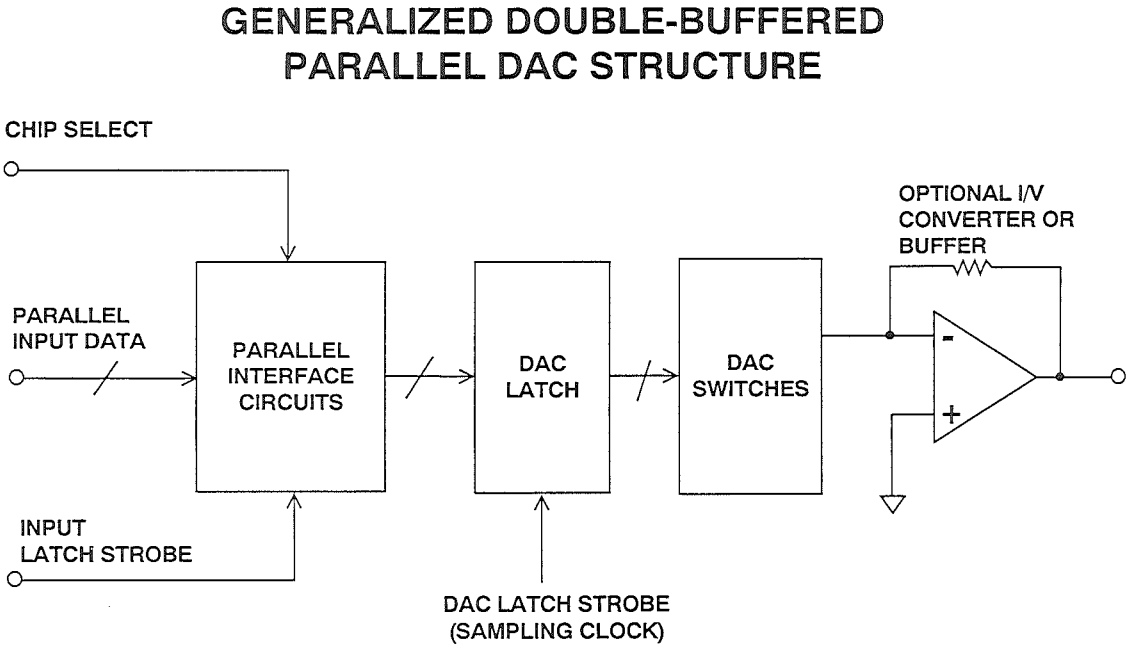


Figure 6.22

The output of a DAC may be a current or a voltage. Fast video DACs are generally designed to supply sufficient output current to develop the required signal levels across resistive loads (generally 150Ω, corresponding to a 75Ω source and load-terminated cable). Other DACs are designed to drive a current into a virtual ground and require a current-to-voltage converter (which may be internal or external). There are some high-impedance voltage-output DACs which require an external buffer in order to drive reasonable values of load impedance.

INTERFACING DSPs TO DACs

A generalized parallel DSP to DAC interface is shown in Figure 6.23. The operation is similar to the parallel DSP to ADC interface described above. In most DSP applications the DAC is operated continuously from a stable sampling clock generator which is external to the DSP. The DAC requires double-buffering because of the asynchronous interface to the DSP. The sequence of events is as follows. Asserting the *Sampling Clock Generator* line clocks the word contained in the DAC Input Latch into the DAC Latch (the latch which drives the DAC switches). This causes the DAC output change to the new value. The *Sampling Clock edge* also interrupts the DSP which then *addresses* the DAC, *enables* the DAC *Chip Select*, and *writes* the next data word into the DAC Input Latch using the *Memory Write* and *Data Bus* lines . The DAC is now ready to accept the next Sampling Clock edge.

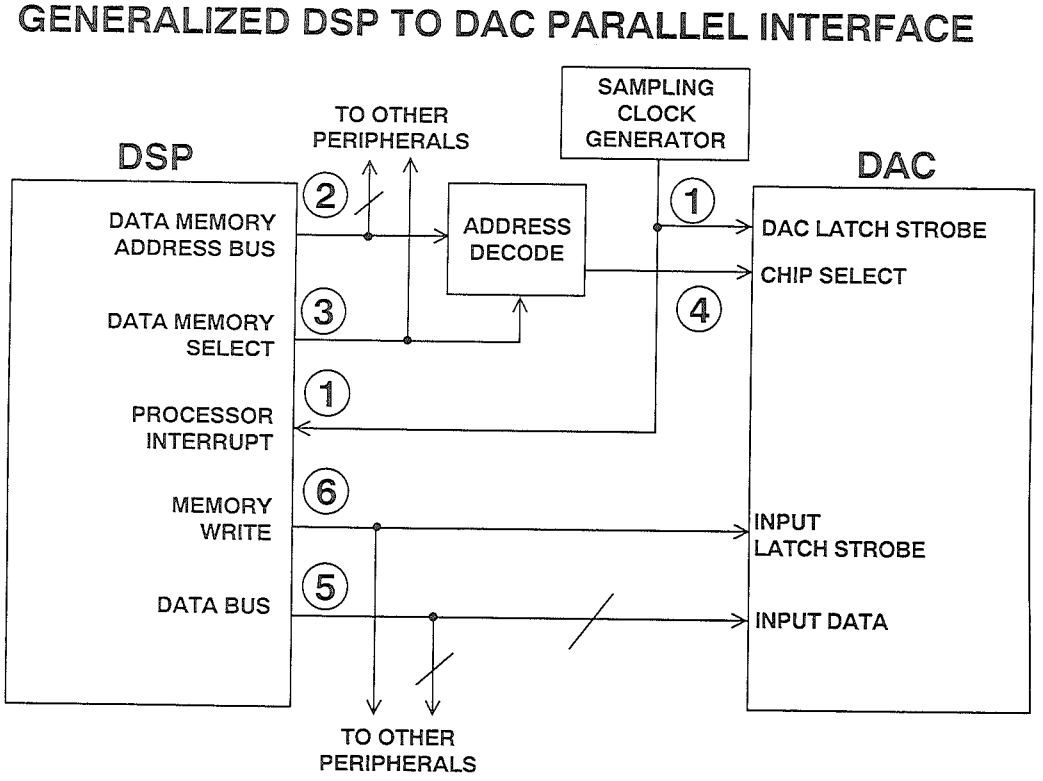


Figure 6.23

A block diagram of a typical serial input DAC is shown in Figure 6.24. The digital input circuitry consists of a serial-to-parallel converter which is driven by a Serial Data line and a Serial Clock. After the serial data is loaded, the DAC Latch Strobe clocks the parallel DAC latch and updates the DAC switches with a new word. Interfacing DSPs to serial DACs is quite easy using the DSP serial port (Figure 6.25). The serial data transfer process is initiated by the assertion of the *Sampling Clock Generator* line. This updates the DAC Latch and causes the Serial Port of the DSP to transmit the next word to the DAC using the *Serial Clock* and the *Serial Data* line.

GENERALIZED SERIAL-INPUT DAC STRUCTURE

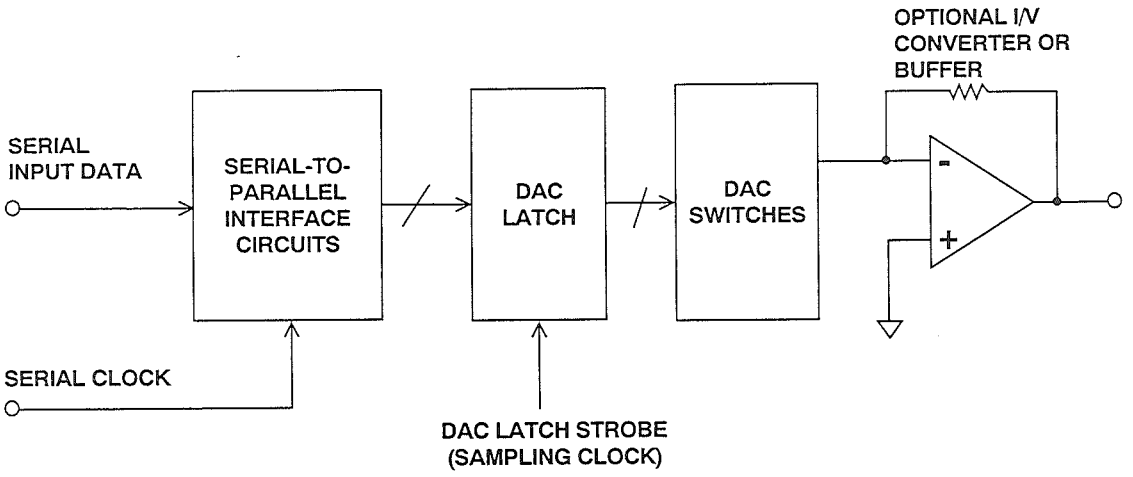


Figure 6.24

GENERALIZED DSP TO DAC SERIAL INTERFACE

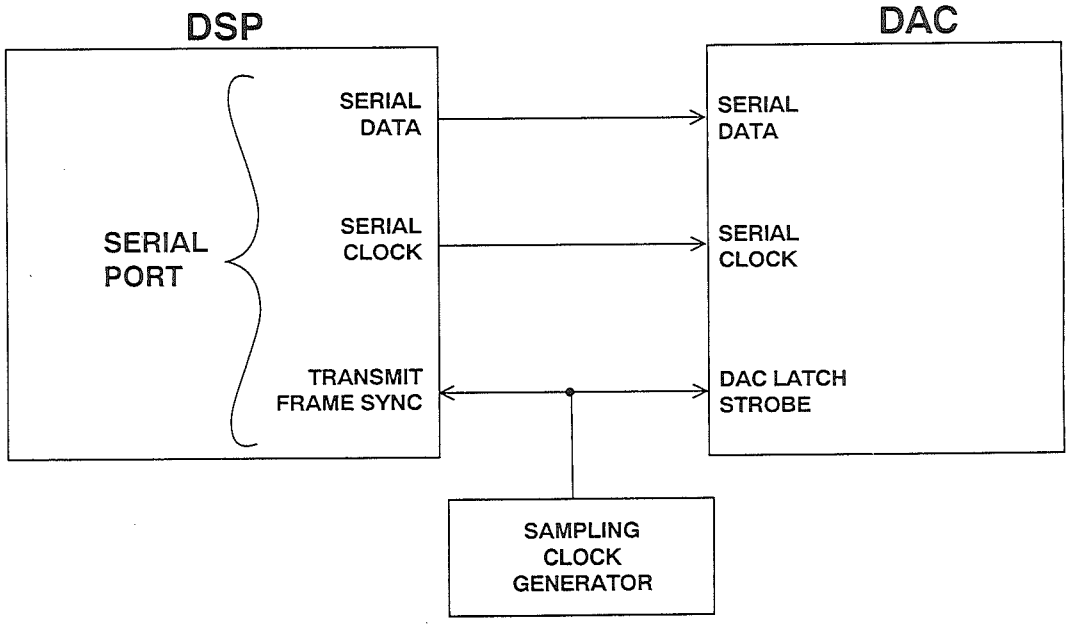


Figure 6.25

BUFFERING DAC OUTPUTS

Whether or not a DAC output requires additional buffering depends upon its structure. Figure 6.26 shows the case of a voltage-output DAC with an external buffer for greater drive capability. The op-amp is connected as a simple follower which may provide additional voltage gain if required.

BUFFERING THE OUTPUT OF A VOLTAGE-OUTPUT DAC

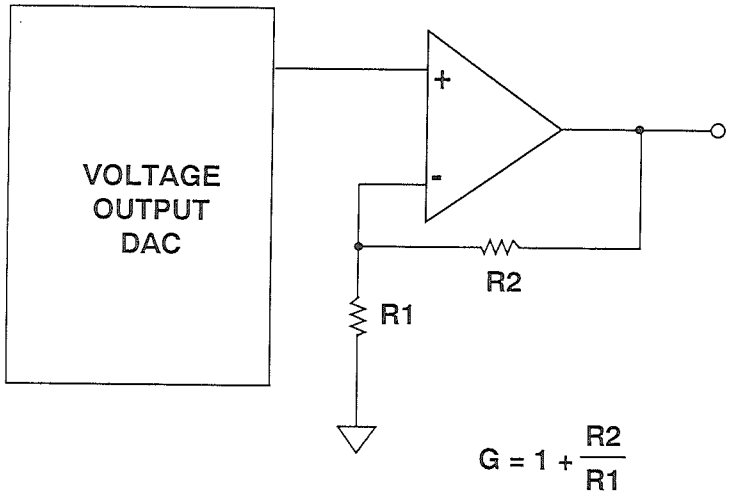
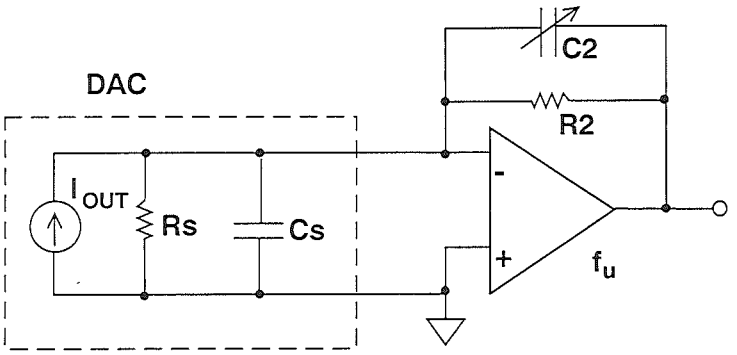


Figure 6.26

A current-output DAC requires a current-to-voltage converter to produce a voltage output. The standard op-amp I/V converter circuit is shown in Figure 6.27. The value of R_2 is chosen to develop the desired voltage for the fullscale DAC output current. C_2 is required to compensate the op-amp because of the additional pole formed by the output capacitance of the DAC, C_S. The value of C_2 is chosen for best frequency and/or pulse response. If the output resistance of the DAC, R_S, and the feedback resistor, R_2, are of the same order of magnitude, the C_2 should be chosen such that $R_2C_2 \approx R_SC_S$.

If, however, $R_S >> R_2$, then C_2 must be chosen in a different manner. The value of C_2 should be chosen such that the phase margin of the two-pole circuit is between 45° and 65°. The actual value should be chosen in the circuit by adjusting C_2 to provide the best tradeoff between frequency and pulse response.

BUFFERING THE OUTPUT OF A CURRENT-OUTPUT DAC



- IF Rs AMD R2 ARE OF THE SAME ORDER OF MAGNITUDE:

  MAKE $R2 \cdot C2 \approx Rs \cdot Cs$

- IF Rs >> R2, OR LARGE Cs:

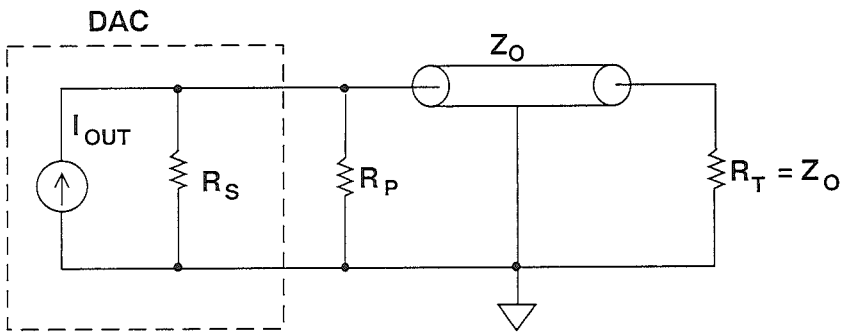
$$\sqrt{\frac{Cs}{2\pi R2 \cdot f_u}} \leq C2 \leq 2\sqrt{\frac{Cs}{2\pi R2 \cdot f_u}}$$

WHERE f_u = OP AMP UNITY GAIN BANDWIDTH PRODUCT

Figure 6.27

Fast, low-glitch DACs such as video-, or DDS DACs often supply a large output current capable of developing sufficient voltage at the output of a source- and load-terminated cable without requiring additional amplification. A typical configuration is shown in Figure 6.28. In order for the cable to be source-terminated, make $R_S \| R_P = Z_O$.

TYPICAL VIDEODAC OUTPUTS REQUIRE NO BUFFERING



$$\text{MAKE } \frac{R_S R_P}{R_S + R_P} = Z_O$$

Figure 6.28

DEGLITCHING DACS USING SHAS

Sample-and-hold circuits can be used to deglitch DACs as shown in Figure 6.29. Just prior to latching new data into the DAC Latch, the SHA is put into the *hold* mode so that the DAC switching glitches are isolated from the output. The transients produced by the SHA are code-independent, occur at the update frequency, and so are easily filtered. However, modern DACs designed for low glitch and high spectral purity generally achieve the required performance without the requirement for an external SHA.

DEGLITCHING A DAC OUTPUT USING A SAMPLE-AND-HOLD

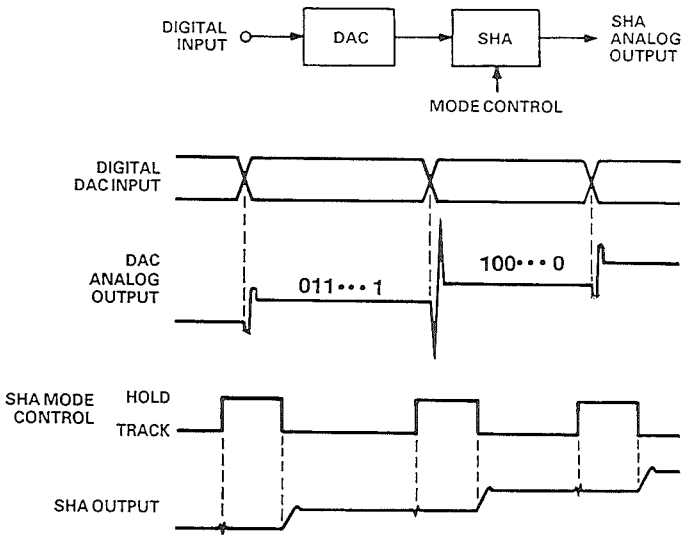


Figure 6.29

Not all sample-and-hold circuits are suitable for this type of application. Some (for example, the AD781) have quite large temperature variable offset in the sample mode, but are very accurate during the hold mode. Only SHAs with low offset in both sample and hold mode are suitable for deglitching DACs.

SIN(x)/x FREQUENCY ROLLOFF EFFECT

The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate (Figure 6.30). The reconstructed signal is down 3.92dB at the Nyquist frequency with respect to the low frequency amplitude. An inverse sin(x)/x filter is sometimes placed after the DAC to correct for this effect and is often incorporated in the anti-aliasing filter.

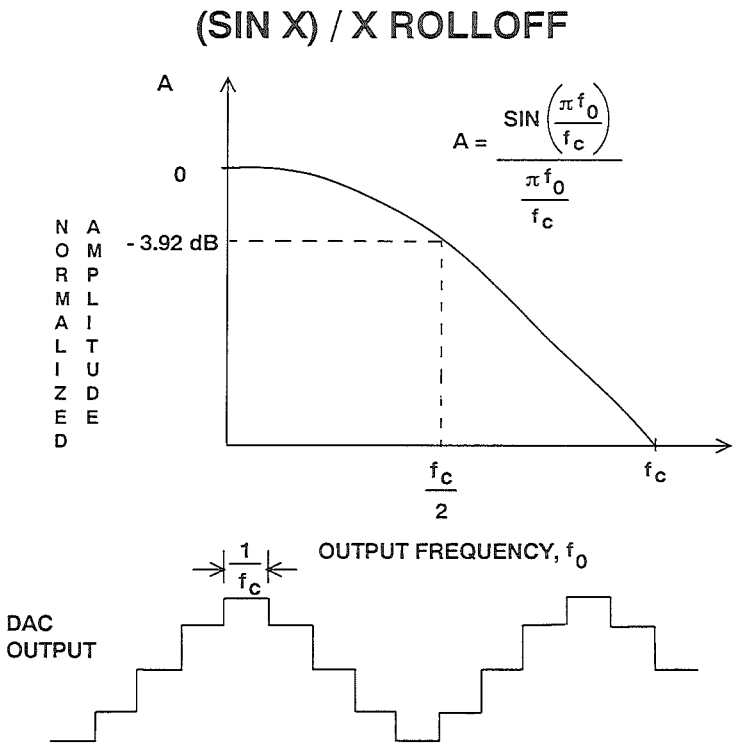


Figure 6.30

SUPPLYING THE REFERENCE VOLTAGE FOR DACs

Like ADCs, many DACs have an internal reference which may be left unused in favor of a more stable, lower-noise external reference. The same considerations previously discussed for ADCs apply to the selection of a DAC reference, including the possibility of the DAC being trimmed to its internal reference voltage, so that the use of a high precision external reference actually gives less DAC accuracy.

REFERENCE VOLTAGES FOR DACs

- DACs may or may not have internal references
- The internal reference (if supplied) is usually not as good as an external one because of process limitations
- An external reference may be substituted for the internal one to achieve higher performance

Figure 6.31

SAMPLING CLOCK GENERATION FOR ADCS AND DACS

Many users of sampling ADCs and DACs fail to understand the critical nature of the sampling clock signal. The tendency is to focus more on the analog input/output signals and treat the sampling clock as just another digital signal. Unfortunately, noise and jitter on the sampling clock input will cause performance degradation in both ADCs and DACs.

Jitter in an ADC, t_a, is simply the rms value of the sample-to-sample variation in the precise point in time at which the input signal is sampled. This rms time jitter produces a corresponding rms voltage error which is proportional to the slew rate of the input signal. The effect of broadband time jitter is to degrade the overall SNR of the ADC.

Jitter for an ADC is usually attributed to the SHA. The ADC aperture jitter, unfortunately, is certainly not the only possible source for this error. In a practical ADC, the sampling clock is often phase and amplitude modulated by some unwanted external sources; the sources can be wideband random noise, oscillator phase noise, power line noise, or digital noise due to poor layout, bypassing, and grounding techniques. Phase jitter on the sampling clock produces the same effect as jitter on the input sinewave.

The effects of even small amounts of timing jitter are shown in Figure 6.32, where SNR and ENOB are plotted as a function of fullscale input sinewave frequency for various amounts of rms timing jitter using the formula shown. For example, in order to achieve 12 bit SNR (74dB) on a 10MHz fullscale input sinewave, the rms jitter can be no more than 3ps rms.

EFFECTS OF APERTURE JITTER ON SNR AND ENOB

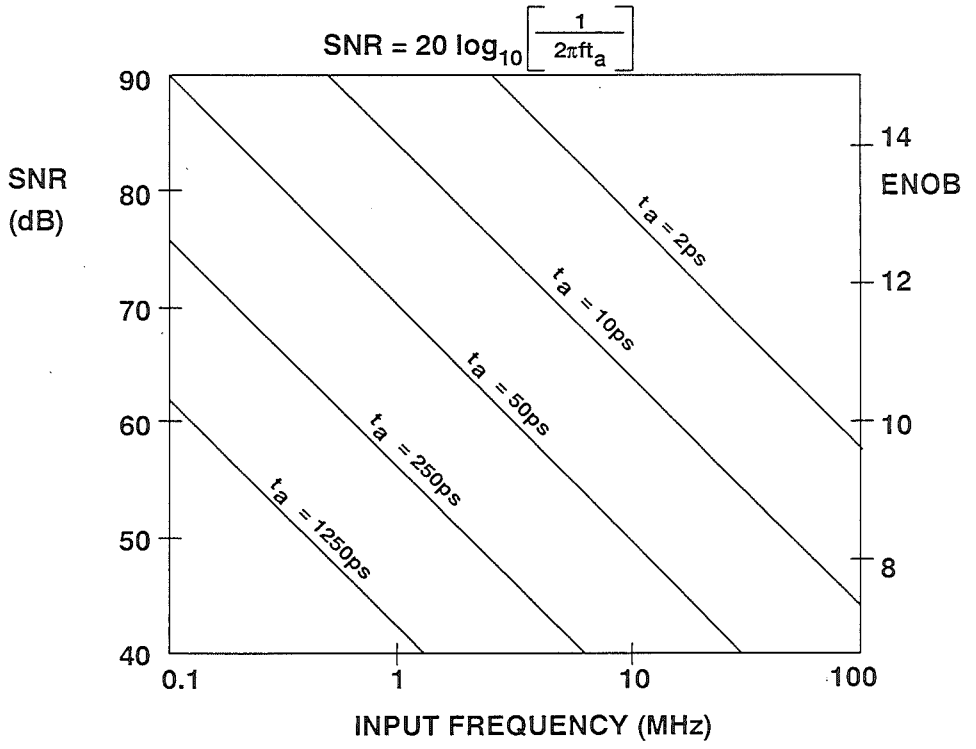


Figure 6.32

The total rms timing jitter will probably consist of two frequency components: narrowband and broadband. The sampling clock oscillator will probably have narrowband phase noise. The effect of narrow-band phase noise centered about the sampling frequency is to produce similar phase noise about the fundamental sinusoid frequency in an FFT of the digitized sinusoid. The high-speed logic circuits in the sampling clock path may introduce broadband noise on the pulse edges which in turn causes broadband jitter due to sample-to-sample variations in the precise times at which the internal logic thresholds are crossed. ECL logic gates have an effective bandwidth greater than 300MHz, and a typical 100K ECL gate has an effective rms timing jitter of approximately 7ps rms.

A detailed mathematical analysis of broadband and narrowband timing jitter is much beyond the scope of this discussion, however their effects may be observed directly in the FFT analysis of a sinusoid. The narrowband phase noise will show up as a widening of the main lobe of the fundamental sinusoid, while the broadband jitter will cause an overall increase in the noise floor.

The sampling clock generator must have low phase noise, therefore RC and relaxation oscillators should be ruled out completely. A crystal oscillator is much preferred. The crystal oscillator should not be constructed out of logic gates, capacitors, and resistors, however, but should be built around discrete bipolar and FET devices in the circuits recommended by the crystal manufacturer. In exacting applications, additional filtering may be required (Figure 6.33). The bandpass filter following the crystal oscillator serves to remove any frequency skirts around the sampling frequency. The lowpass filter then removes any harmonics of the sampling clock frequency which may not have adequately been attenuated by the bandpass filter. The output then drives a low-jitter wideband comparator which converts the sinewave into a digital signal. Use a TTL comparator such as the AD9696 if the ADC requires TTL inputs, or an ECL comparator such as the AD96685 if ECL inputs are required.

The sampling clock circuits themselves should be isolated as much as possible from the noise present in the digital portions of the system. Separate decoupled power supplies may also be required for optimum results. It is extremely important that the digital outputs of the ADC (and digital inputs to a DAC) not be allowed to couple into the sampling clock signal. Coupling will cause an increase in the harmonic distortion of due to signal-dependent digital transients coupling into the sampling clock. On the other hand, the sampling clock is itself a digital signal. It has the potential for causing noise in the analog portion of the system. It should therefore be isolated from both the analog and digital portions of the system. As we will see in the next section, the sampling clock generator circuits should be referenced and decoupled to the analog ground plane.

GENERATING PRECISION LOW-JITTER SAMPLING CLOCKS

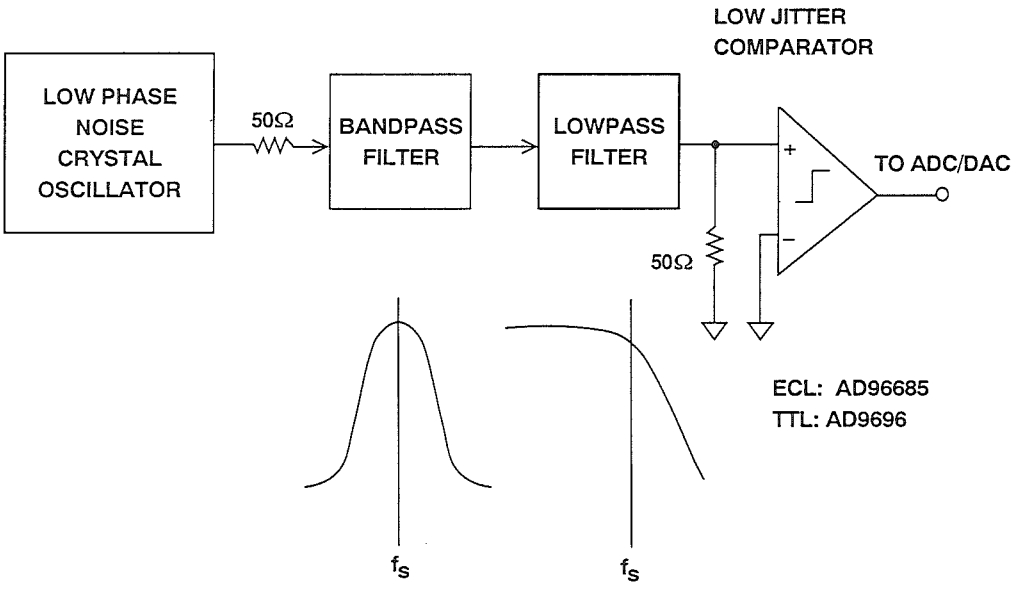


Figure 6.33

POWER SUPPLIES, GROUND PLANES, DECOUPLING, AND LAYOUT

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

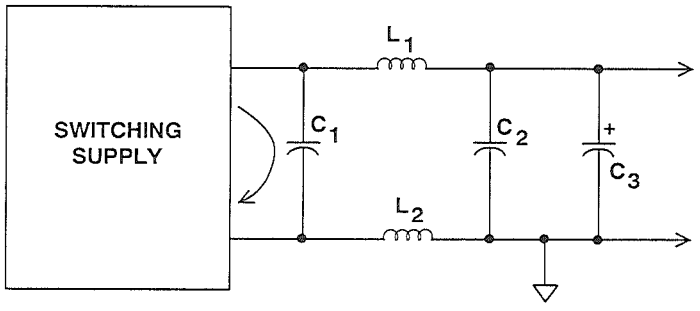
Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.

SWITCHING-MODE POWER SUPPLIES

- Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)
- Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits
- Optimum Filter Design Depends on Power Supply Characteristics. Beware of Power Supply Design Changes.
- Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields
- Physically Isolate Supply from Analog Circuits
- Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise

Figure 6.34

FILTERING A SWITCHING SUPPLY OUTPUT



- C_1 MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- C_2 IS ALSO LOW INDUCTANCE, C_3 IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED, L_2 SHOULD BE OMITTED

Figure 6.35

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 6.35 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.

Proper power supply decoupling techniques must be used on each PC board in the system. Figure 6.36 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL and low ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and 5μF). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!

PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO ACHIEVING GOOD HIGH SPEED SYSTEM PERFORMANCE

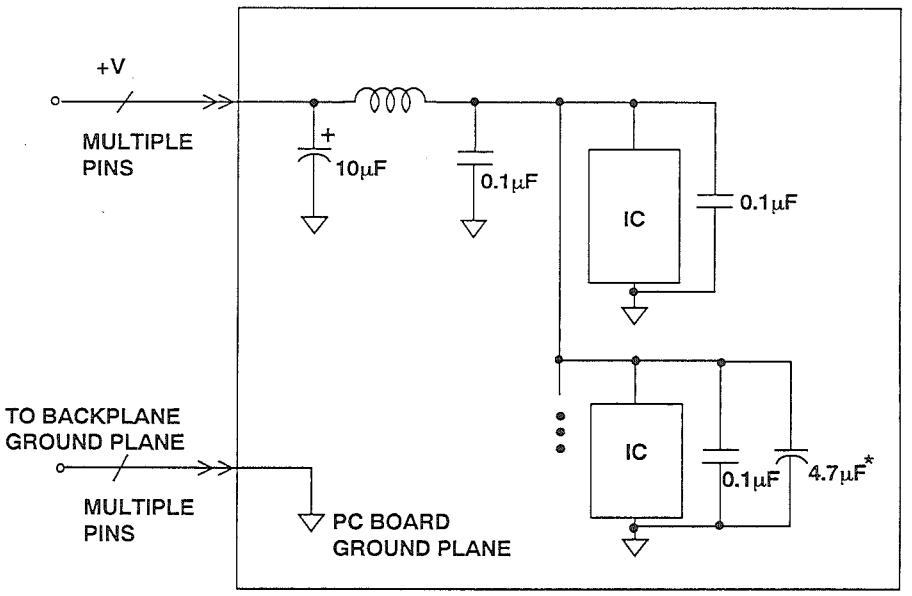


Figure 6.36

If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multicard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 6.37. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system *star ground* , or *single-point ground*, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent accidental dc voltages from developing between the two ground systems.

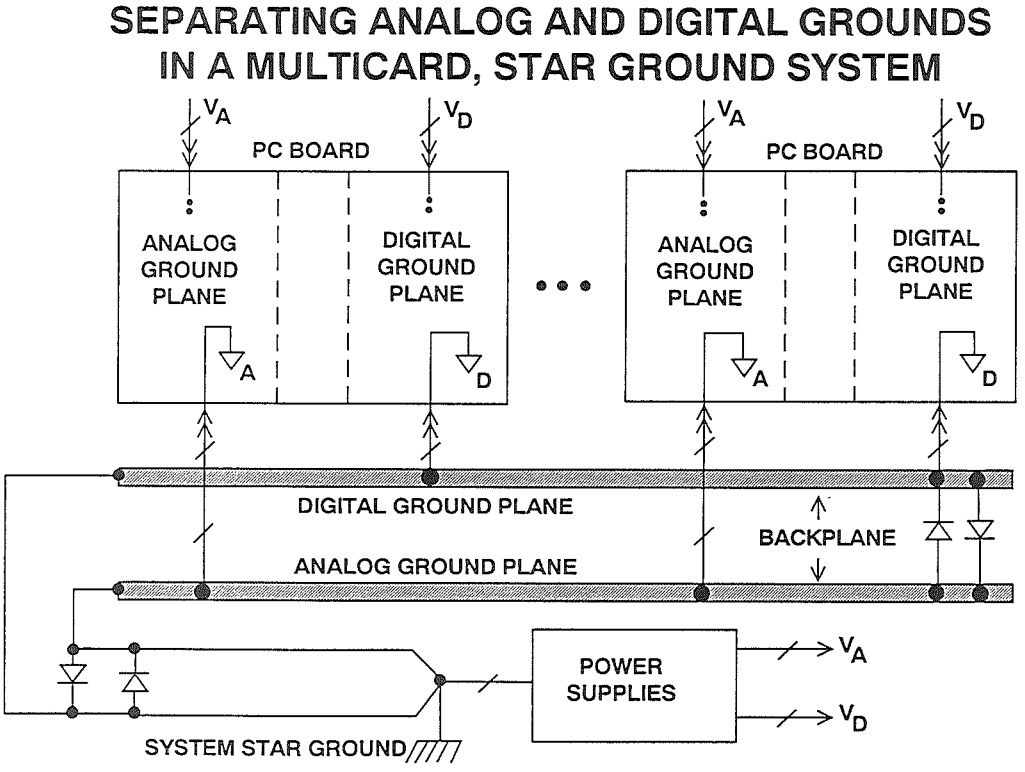


Figure 6.37

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 6.38 will help to explain this seeming dilemma.

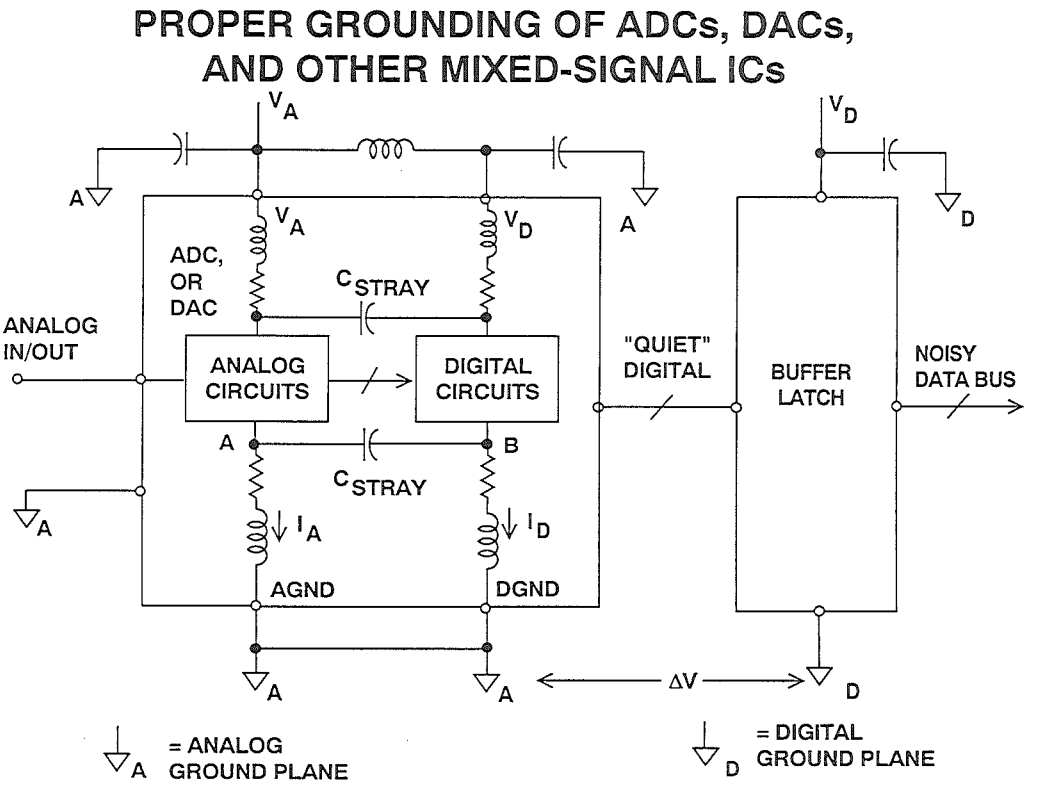


Figure 6.38

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 6.38 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. the rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of

the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. It does not say that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout. Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 6.38. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 6.38) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A clean, analog-grade supply can be generated from a 5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 6.40. The supply output is virtually free of any glitch noise as evident in the scope photo shown in Figure 6.41, which compares the input and output sides of the filter. All capacitors were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors. The circuit as

shown can handle 100mA of load current without the risk of saturating the ferrite core. Higher current capacity can be achieved using larger ferrite cores.

POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS

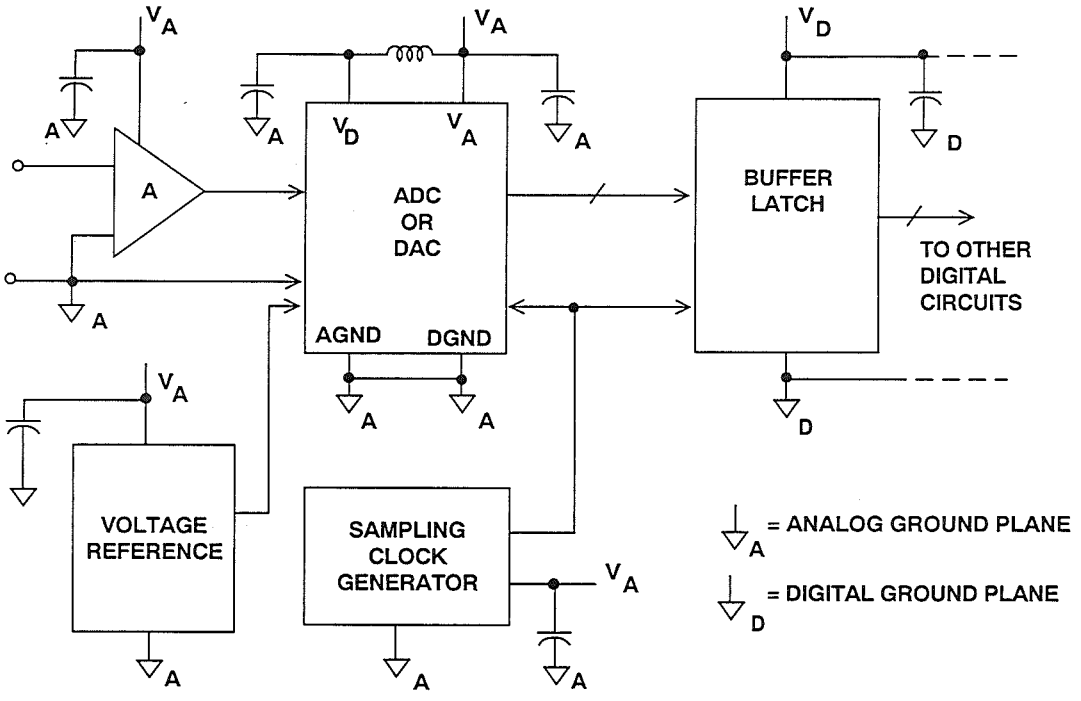


Figure 6.39

DIFFERENTIAL LC FILTER TURNS NOISY LOGIC SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

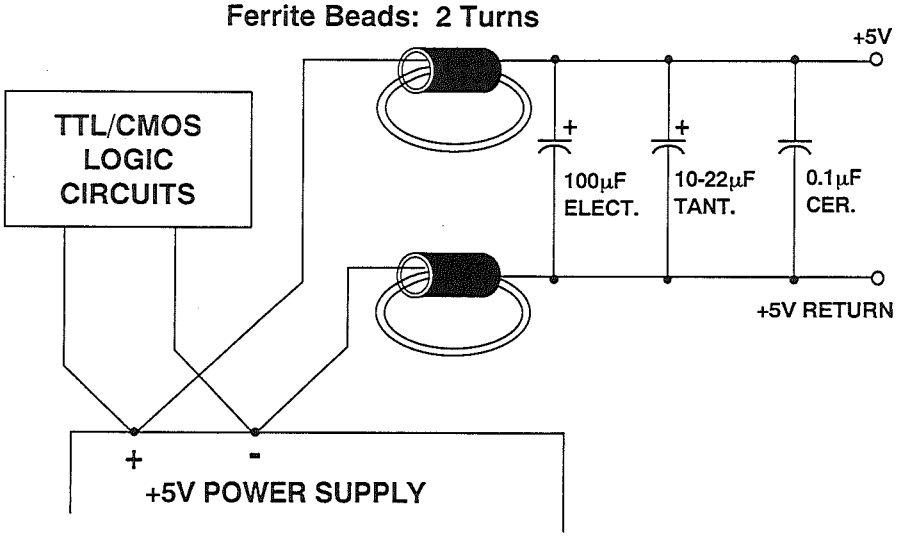
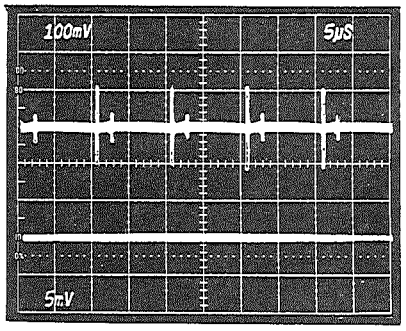


Figure 6.40

LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE

BEFORE FILTER

AFTER FILTER



100mV / div.

5mV / div.

HORIZONTAL SCALE: 5µs / div.

Figure 6.41

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC/DAC analog runs.
- Use lots of ground plane.
- Use microstrip techniques at high frequencies for controlled impedances and controlled return current paths.
- Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.

Figure 6.42

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 6.43 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

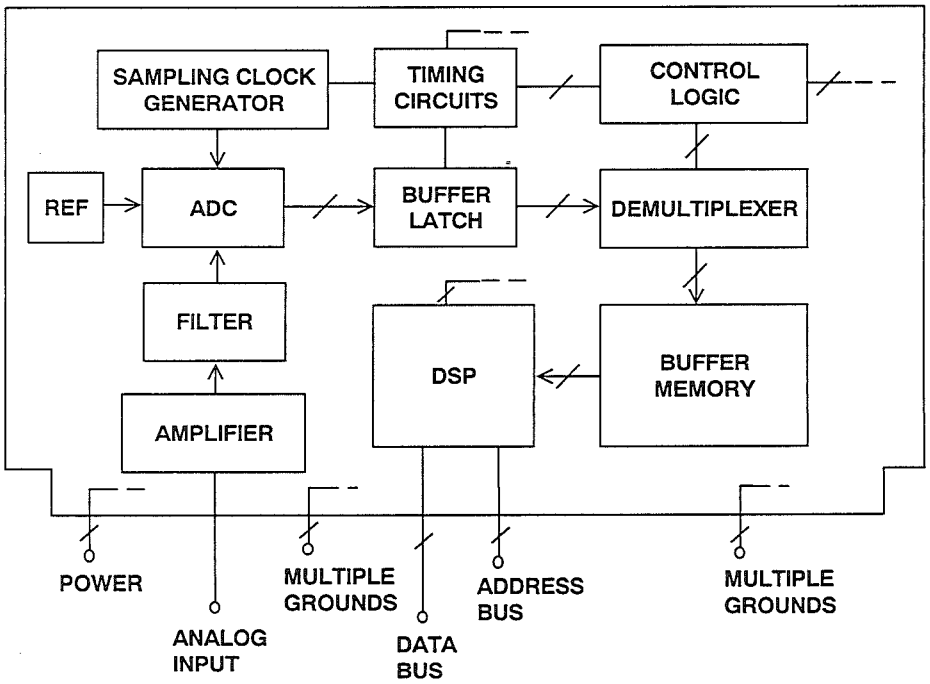


Figure 6.43

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

EDGE CONNECTIONS

- Separate sensitive signal by ground pins.
- Keep down ground impedances with multiple (30-40% of total) ground pins.
- Have several pins for each power line.
- Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.

Figure 6.44

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

SOCKETS

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- DON'T! (If at all possible)
- Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).
- Always test the effect of sockets by comparing system performance with and without the use of sockets.
- Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.

Figure 6.45

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be

avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. This approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multicard system.

PROTOTYPING MIXED SIGNAL CIRCUITRY

- NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).
- Wherever possible avoid the use of sockets for analog ICs.
- Use a prototype of your final PCB layout as early as possible.

Figure 6.46

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient this is not essential), with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in Reference 1 at the end of this section.

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 6.47

REFERENCES

1. Wainwright Instruments, Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel. 619-558-1057. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-5174.

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