Evaluation of the ADRF5238 High Isolation, Silicon SPDT, Nonreflective Switch, 0.1GHz to 13GHz

FEATURES

- Full-featured evaluation board for the ADRF5238
- Easy connection to the test equipment
- Thru line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5238 is a SPDT switch manufactured in the silicon process.

This user guide describes the ADRF5238-EVALZ evaluation board, designed to evaluate the features and performance of the ADRF5238. Figure 1 shows a photograph of the evaluation board.

Full specifications on the ADRF5238 are available in the ADRF5238 data sheet from Analog Devices, Inc. Consult the data sheet with this user guide when using the ADRF5238-EVALZ evaluation board.

ADRF5238-EVALZ EVALUATION BOARD PHOTOGRAPH

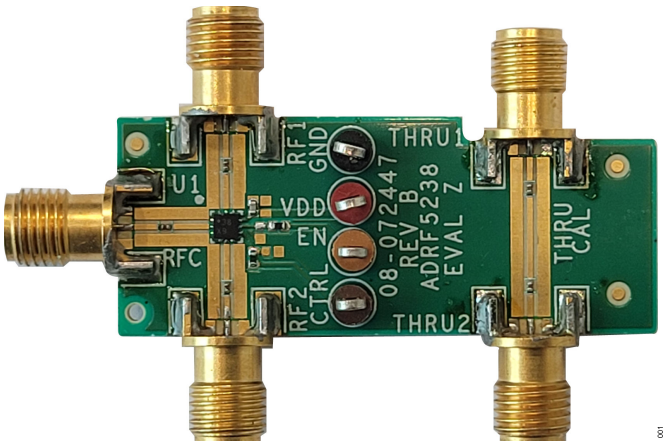

Figure 1. ADRF5238-EVALZ Evaluation Board Photograph

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REVISION HISTORY

12/2024—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5238-EVALZ is a connectorized board, assembled with the ADRF5238 and its application circuitry. All components are placed on the primary side of the ADRF5238-EVALZ. An assembly drawing for the ADRF5238-EVALZ is shown in Figure 6, and an evaluation board schematic is shown in Figure 5.

BOARD LAYOUT

The ADRF5238-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

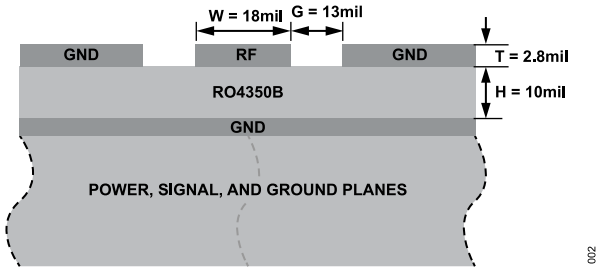

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 2.8mil thick, and the inner layers are 1.4mil thick.

All RF and DC traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 10mil Rogers RO4350B, offering optimal high-frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62mil, which allows edge launch RF connectors to be placed at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 18mil and a ground spacing of 13mil to have a characteristic impedance of 50Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5238, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5238-EVALZ has one power-supply input, two control inputs, and a ground, as shown in Table 1. The DC test points are populated on GND, VDD, EN, and CTRL. The ground reference must be connected to GND. The power supply (3.3V to 5V) is connected to the DC test point on VDD. Control inputs, EN and CTRL, are connected to 3.3V or 0V. The typical supply current consumption for the ADRF5238 is 400µA with a 5V supply and 200µA with a 3.3V supply voltage.

The VDD supply pin of the ADRF5238 are decoupled with 100pF capacitor.

Table 1. Power-Supply and Control Inputs

Test Points	Description
V_{DD}	Positive supply voltage
CTRL	Control input voltage
EN	Enable input voltage
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5238-EVALZ has five edge-mounted, 2.92mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92mm Connectors	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
THRU1	Thru line input and output
THRU2	Thru line input and output

The through calibration line, connecting the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5238-EVALZ to determine the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5238-EVALZ at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5238.

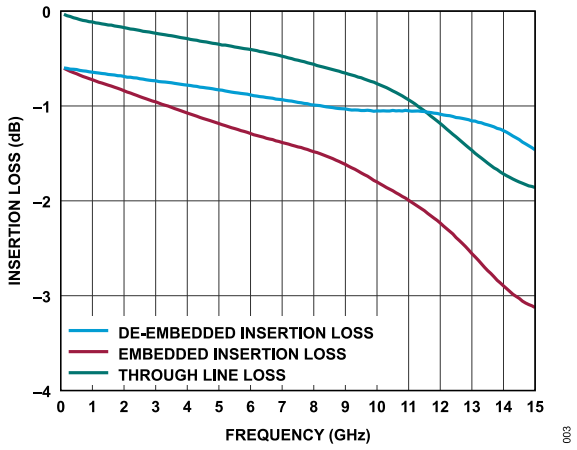

Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5238-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the CTRL test point.
4. Bias up the EN test point.
5. Apply an RF input signal.

The ADRF5238-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the ADRF5238-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage-output terminal of the 3.3V to 5V supply.
3. Connect the CTRL test point to the voltage-output terminal of the 3.3V supply. The ADRF5238 can be configured in different modes by connecting the CTRL test point to 3.3V or 0V, as shown in Table 3.
4. Connect the EN test point to the voltage-output terminal of the 3.3V supply. The ADRF5238 can be configured in different modes by connecting the EN test point to 3.3V or 0V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, and RF2 2.92mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50Ω. Sweep the frequency from 10MHz to 15GHz and set the power to –10dBm.

Additional test equipment is required to fully evaluate the functions and performance of the ADRF5238.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high-isolation power combiner is also recommended.

For power compression evaluation and power handling evaluation, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92mm connectors of the ADRF5238-EVALZ include the losses of the 2.92mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5238-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the ADRF5238-EVALZ and equal in length.

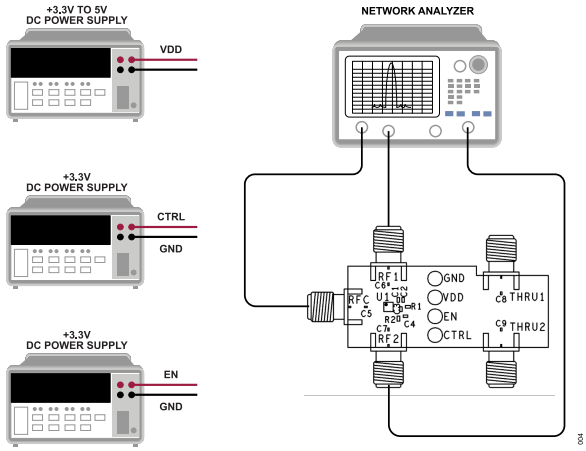

Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

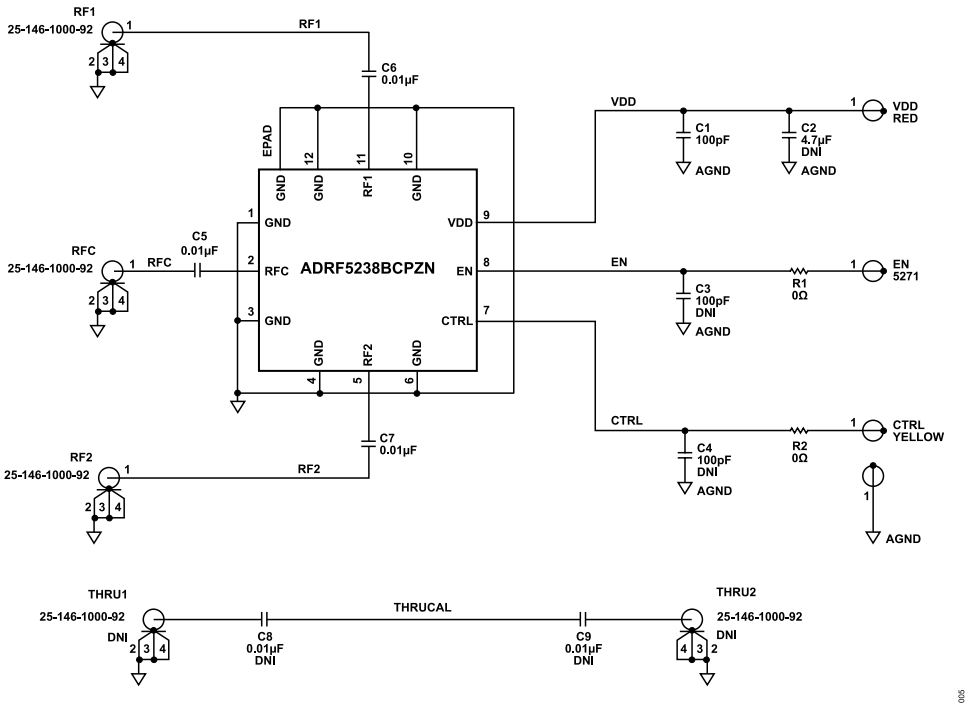

Figure 5. ADRF5238-EVALZ Evaluation Board Schematic

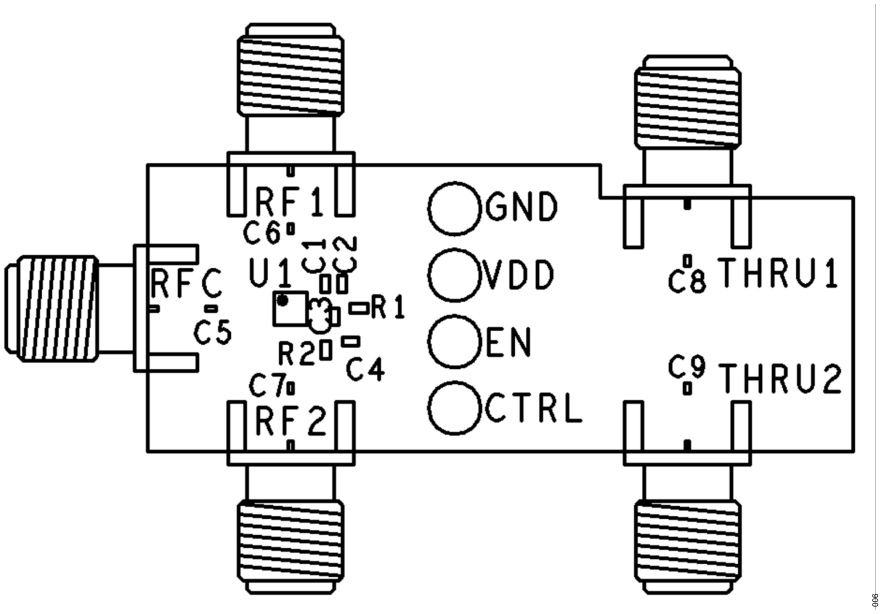

Figure 6. ADRF5238-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5238-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
2	R1, R2	0Ω resistors, surface-mounted device (SMD), jumper, 1/8W, 0402	Vishay	RCC04020000Z0ED
1	C1	100pF ceramic capacitor, 50V, 5%, C0G, 0402	Murata	GCM1555C1H101JA16D
3	C5, C6, C7	0.01µF ceramic capacitors, 25V, 10%, X7R, 0201	Passive Plus Inc.	0201BB103KW250
4	CTRL, EN, VDD, GND	Connector, PCB test points	Keystone	5xxx
3	RFC, RF1, RF2	Edge-mount 2.92mm connectors	SRI Connector Gage Co.	25-146-1000-92
1	U1	High isolation, silicon SPDT, nonreflective switch, 0.1GHz to 13GHz	Analog Devices, Inc	ADRF5238BCPZN
1	PCB	ADRF5238-EVALZ	Analog Devices	BR-072447b
1	C2	4.7µF ceramic capacitor, 16V, 20%, X5R, 0402, do not install (DNI)	Samsung	CL05A475MO5NUNC
2	C3, C4	100pF ceramic capacitors, 50V, 5% C0G, 0402, DNI	Murata	GCM1555C1H101JA16D
2	C8, C9	0.01µF ceramic capacitors, 25V, 10%, X7R, 0201, DNI	Passive Plus Inc.	0201BB103KW250
2	THRU1, THRU2	Edge-mount 2.92mm connectors, DNI	SRI Connector Gage Co.	25-146-1000-92

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.