Evaluation Board User Guide

ADPL42002 Evaluation Boards

Evaluate: ADPL42002

General Description

The ADPL42002 evaluation boards evaluate the ADPL42002, a 20V, 200mA, low noise, CMOS, low dropout (LDO) linear regulator.

See the *Ordering Information* section for the two types of evaluation boards available to evaluate the ADPL42002. One board features a 6-lead, 2mm x 2mm LFCSP package, while the other utilizes an 8-lead SOIC package.

The evaluation boards provide a 3.3V output over an input range of 3.8V to 20V. The maximum output current is 200mA, but output current is also limited by the thermal dissipation of the ADPL42002. The evaluation boards use the adjustable version of the ADPL42002. A resistor divider programs the output of the adjustable ADPL42002 to 3.3V. Noise performance for the adjustable ADPL42002 can be made comparable to a fixed output ADPL42002 by installing optional RC network components into the placeholders that the evaluation board printed circuit board (PCB) designs provide. The evaluation boards can easily be configured with a jumper for fixed output versions of the ADPL42002 that normally have their SENS/ADJ pin connected directly to the output.

In addition to connectors for the input voltage, output voltage, EN control signal and ground, the evaluation boards provide test points for the input, output, and SS pin (for the LFCSP package) voltages. A jumper normally connects the EN pin to the V_{IN} input, but the jumper can be repositioned so EN can be driven externally at its connector instead. A pull-down resistor is also connected to the EN pin to drive the pin low when the device needs to be turned off.

For more details, refer to the ADPL42002 data sheet, which must be consulted in addition to this user guide when using the ADPL42002 evaluation boards.

Features and Benefits

- Input Voltage Range: 3.8V to 20V
- Resistor Programmed: 3.3V Output Voltage
- Maximum Output Current: 200mA
- Jumper Turns Regulator ON or Connects the EN Pin to a Connector to Turn the Regulator ON or OFF Externally
- Jumper Connects the SENSE/ADJ Pin to the Output Through a Resistor Divider or Directly
- V_{IN}, V_{OUT}, and GND Test Points for Regulations and Dropout Voltage Monitoring
- Component Placeholders for an RC Network that can Reduce Noise when the SENSE/ADJ Pin Connects to the Output Through a Resistor Divider
- Component Placeholder for a Soft-Start Capacitor
- SS Test Point for Soft-Start Voltage Monitoring -LFCSP Package Evaluation Board Only
- 6-Lead (2mm x 2mm) LFCSP Package or an 8-Lead SOIC Package

***Ordering Information* appears at end of data sheet.**

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

Quick Start

Required Equipment

- A DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

Procedure

The ADPL42002 evaluation boards are simple to set up to evaluate the performance of the ADPL42002. See *Figure 1* or *Figure 2* for the evaluation board connections, and take the following steps:

1. Connect the load between the V_{OUT} and GND terminals.
2. With the input power supply off and turned down, connect the input supply to the V_{IN} and GND terminals. Ensure that the shunt of JP1 connects EN to V_{IN} according to the jumper connection guide. Also ensure that the shunt of JP2 allows the resistor divider to program the output to 3.3V according to the jumper connection guide.
3. With the load turned down, turn the input power supply on and increase the voltage to 3.8V or higher.
4. Vary V_{IN} from 3.8V to 20V and the load current from 0A to 200mA. Observe conservative power dissipation limits and note the following when setting V_{IN} and the load current:
   - An input voltage that is too close to the programmed output voltage (too low) can cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
5. Monitor regulation and dropout voltage at the V_{IN}, V_{OUT}, and GND test points.
6. To apply an EN signal externally, reposition jumper JP1 and apply the EN signal to the EN connector.
7. If an output voltage other than 3.3V is desired, change resistors R1 and R2.
8. An RC network can be installed in the component placeholder locations in parallel with the top feedback divider resistor R1 to improve noise performance. Refer to the ADPL42002 data sheet for details.
9. JP2 is a convenient way to connect the SENSE/ADJ pin directly to the output if a fixed-output ADPL42002 is installed. The bottom feedback divider resistor R2 may be removed as well.
10. A soft-start capacitor can be installed in the C3 placeholder. On the LFCSP package version evaluation board only, monitor the soft start voltage at the SS test point.

Evaluation Board Photos

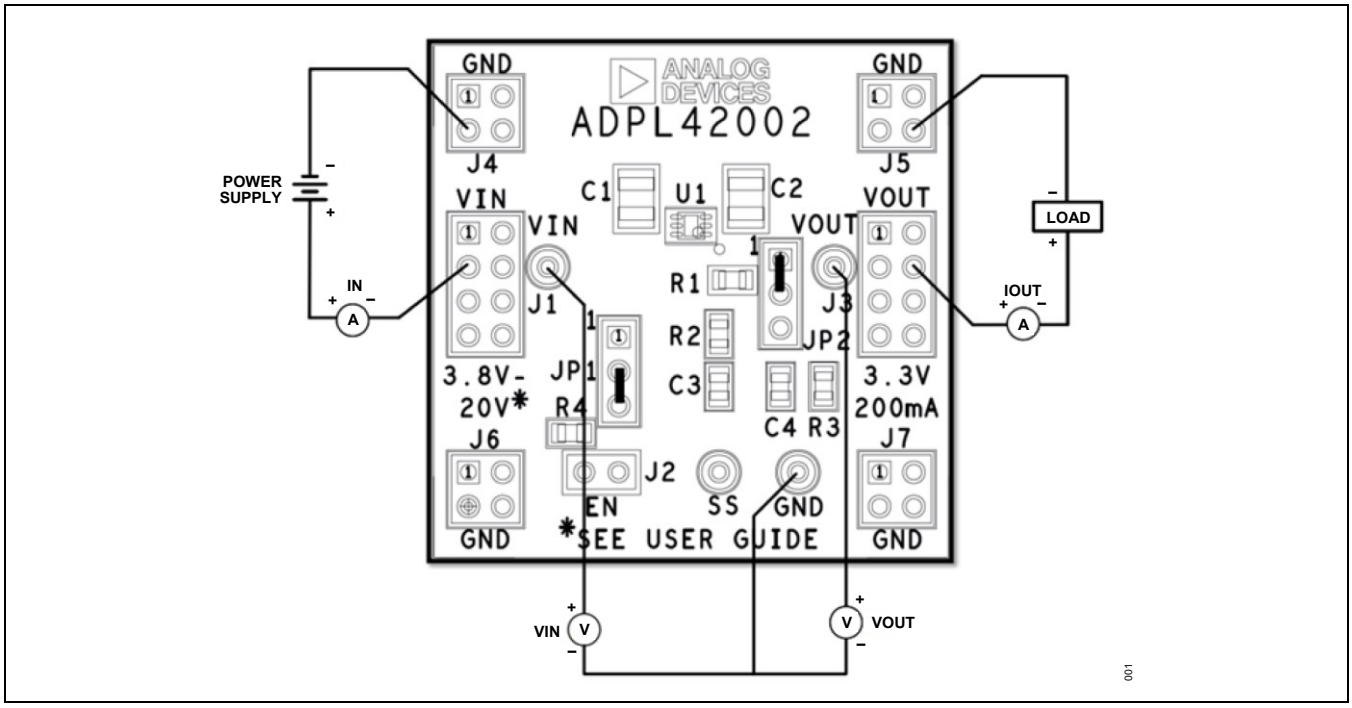


Figure 1. LFCSP Package Evaluation Board Connection

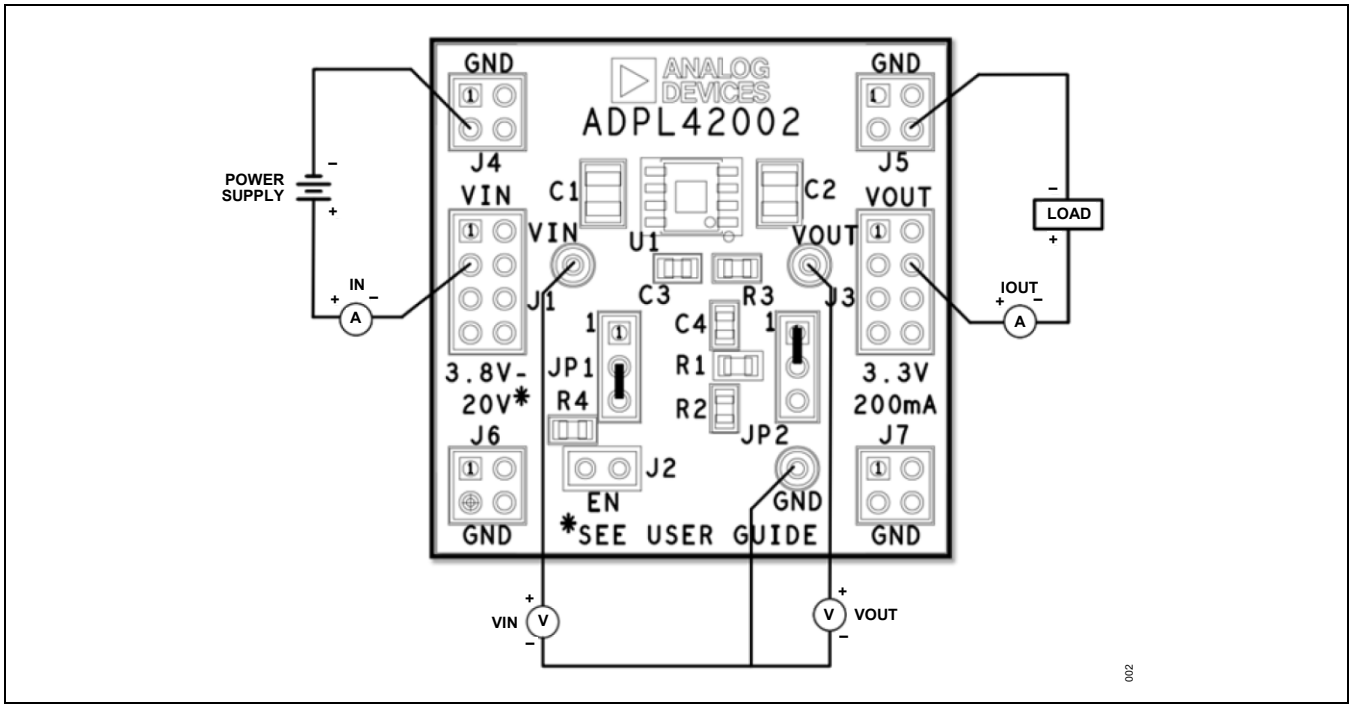


Figure 2. SOIC Package Evaluation Board Connection

Performance Summary

Specifications are at T_A = +25°C, unless otherwise noted.

Table 1. Performance Summary of the LFCSP Package Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 10mA, V_{OUT} = 3.3V	3.8		20	V
		I_{OUT} = 200mA, V_{OUT} = 3.3V	3.8		7.8[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 200mA, R1 = 17.4kΩ, R2 = 10kΩ	3.22	3.29	3.36	V
Feedback Divider Current	I_{FB}	JP1 = pins 2-3, JP2 = pins 1-2, R1 = 17.4kΩ, R2 = 10kΩ		120		µA
Shutdown Input Current	I_{GND_SD}	JP1 = pins 1-2, V_{IN} = 4.3V, EN = GND		1.8		µA

[1] *The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to 3.3V with a 200mA load is determined by the 60°C temperature rise of the ADPL42002 on the evaluation board. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the ADPL42002 data sheet for more information.*

Table 2. Performance Summary of the SOIC Package Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 10mA, V_{OUT} = 3.3V	3.8		20	V
		I_{OUT} = 200mA, V_{OUT} = 3.3V	3.8		9.47[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 200mA, R1 = 17.4kΩ, R2 = 10kΩ	3.22	3.29	3.36	V
Feedback Divider Current	I_{FB}	JP1 = pins 2-3, JP2 = pins 1-2, R1 = 17.4kΩ, R2 = 10kΩ		120		µA
Shutdown Input Current	I_{GND_SD}	JP1 = pins 1-2, V_{IN} = 4.3V, EN = GND		1.8		µA

[1] *The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to 3.3V with a 200mA load is determined by the 60°C temperature rise of the ADPL42002 on the evaluation board. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the ADPL42002 data sheet for more information.*

Printed Circuit Board (PCB) Layout

The printed circuit boards (PCBs) for these evaluation boards are 0.062 inches thick and 1.5 inches square. There are two copper layers, and the finished copper thickness is 1 ounce. The input capacitor, ADPL42002, and output capacitor are all placed on the top side of the PCB. The input and output capacitors are placed near the ADPL42002 with their ground terminals close to each other. The input capacitor, output capacitor, and ADPL42002 grounds all connect on one side of the device, while grounds for control signals connect to the ADPL42002 on the other side of the device. The bottom side of the PCB is a solid ground plane that connects to the ground on the top PCB layer by thermal vias under or near the ADPL42002 and at other points. Layout may significantly affect circuit electrical performance and reliability.

Jumper Connection Guide

JUMPER	DEFAULT CONECTION	FEATURE
JP1	Pin 2-3	Turns Regulator On
JP2	Pin 1-2	Connects the SENSE/ADJ pin to the output through a resistor divider

Ordering Information

MODEL[1], [2]	PACKAGE DESCRIPTION
EVAL-ADPL42002CP-AZ	LFCSP Package Evaluation Board
EVAL-ADPL42002RD-AZ	SOIC Package Evaluation Board

[1] *Z = RoHS Compliant Part*

[2] *The evaluation boards are preconfigured with an adjustable ADPL42002.*

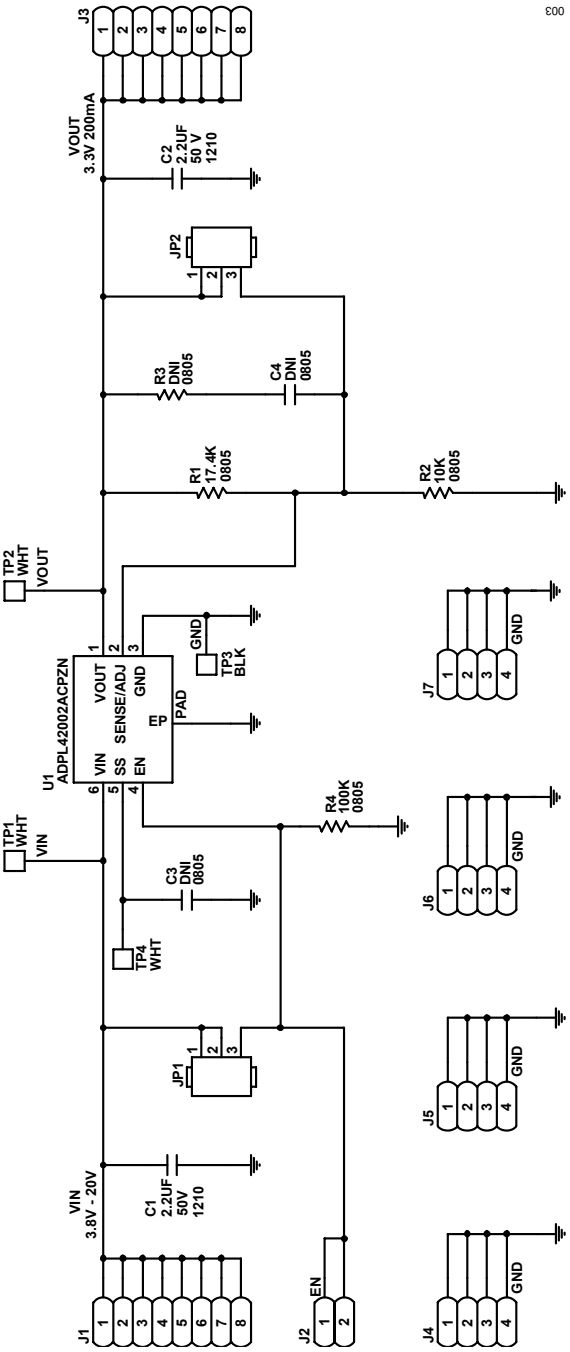
LFCSP Package Evaluation Board Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	2	C1, C2	2.2µF Capacitor, X7R, 50V 10% 1210, soft termination	TDK, C3225X7R1H225K200AE
2	1	R1	17.4kΩ Resistor, 1%, 1/8W, 0805, AEC-Q200	VISHAY, CRCW080517K4FKEA
3	1	R2	10kΩ Resistor, 1%, 1/2W, 0805, AEC-Q200	VISHAY, CRCW080510K0FKEAHP
4	1	R4	100kΩ Resistor, 1%, 1/2W, 0805, AEC-Q200	VISHAY, CRCW0805100KFKEAHP
5	1	U1	20V, 200mA, Low noise, CMOS, LDO Linear Regulator	Analog Devices Inc., ADPL42002ACPZN-R7
Optional Evaluation Board Components				
1		C3, C4	Capacitor, 0805, Optional	
2		R3	Resistor, 0805, Optional	
Hardware				
1	2	J1, J3	Connector, header, male, 2 x 4, 2.54mm, vertical, straight, through hole	SULLINS, PEC04DAAN
2	1	J2	Connector, header, male, 1 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02SAAN
3	4	J4 to J7	Connector, header, male, 2 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02DAAN
4	2	JP1, JP2	Connector, header, male, 1 x 3, 2.54mm, vertical, straight, through hole	SULLINS, PEC03SAAN
5	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2.54mm	SULLINS, SPC02SYAN

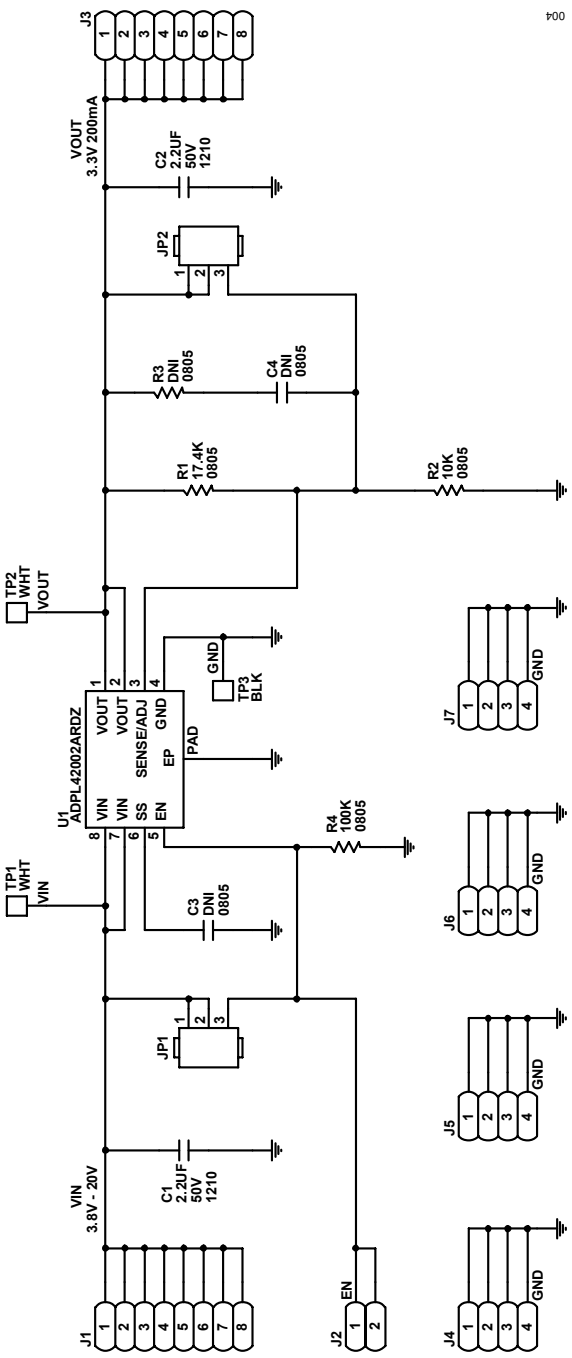
SOIC Package Evaluation Board Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	2	C1, C2	2.2µF Capacitor, X7R, 50V 10%, 1210, soft termination	TDK, C3225X7R1H225K200AE
2	1	R1	17.4kΩ Resistor, 1%, 1/8W, 0805, AEC-Q200	VISHAY, CRCW080517K4FKEA
3	1	R2	10kΩ Resistor, 1%, 1/2W, 0805, AEC-Q200	VISHAY, CRCW080510K0FKEAHP
4	1	R4	100kΩ Resistor, 1%, 1/2W, 0805, AEC-Q200	VISHAY, CRCW0805100KFKEAHP
5	1	U1	20V, 200mA, Low noise, CMOS LDO Linear Regulator	Analog Devices Inc., ADPL42002ARDZ-R7
Optional Evaluation Board Components				
1		C3, C4	Capacitor, 0805, Optional	
2		R3	Resistor, 0805, Optional	
Hardware				
1	2	J1, J3	Connector, header, male, 2 x 4, 2.54mm, vertical, straight, through hole	SULLINS, PEC04DAAN
2	1	J2	Connector, header, male, 1 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02SAAN
3	4	J4 to J7	Connector, header, male, 2 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02DAAN
4	2	JP1, JP2	Connector, header, male, 1 x 3, 2.54mm, vertical, straight, through hole	SULLINS, PEC03SAAN
5	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2.54mm	SULLINS, SPC02SYAN

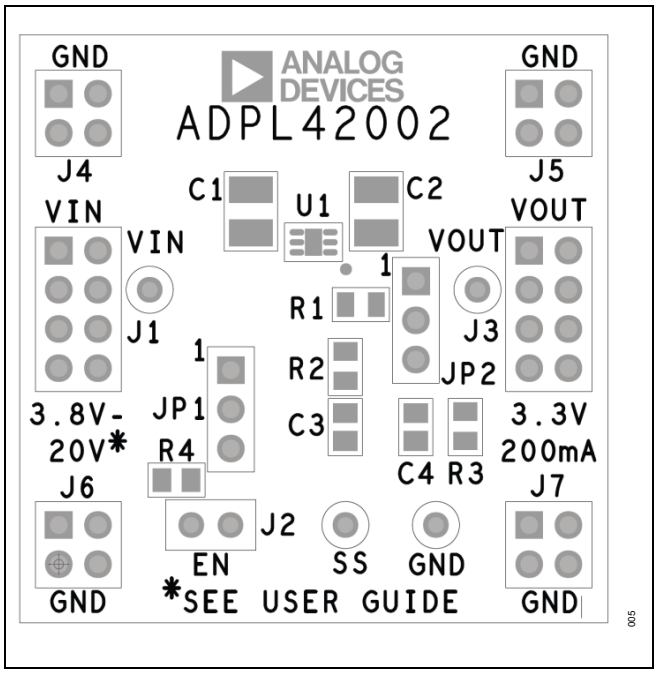
LFCSP Package Evaluation Board Schematic



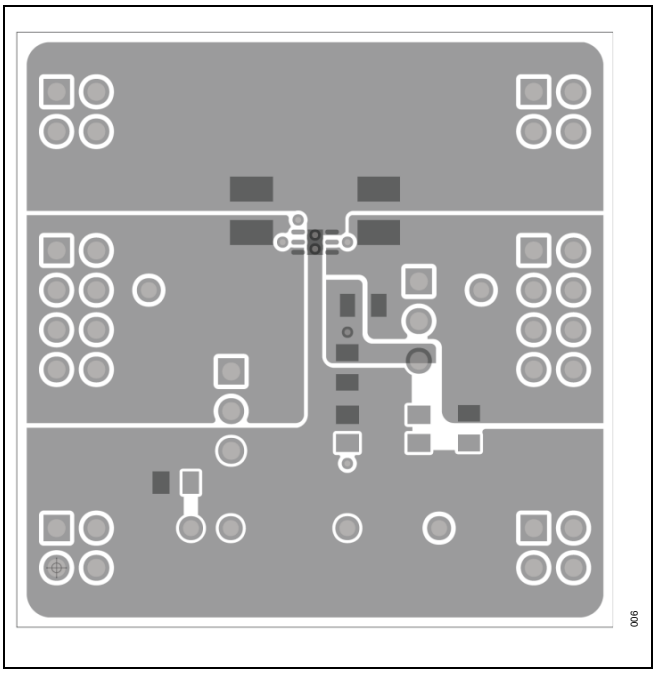
SOIC Package Evaluation Board Schematic



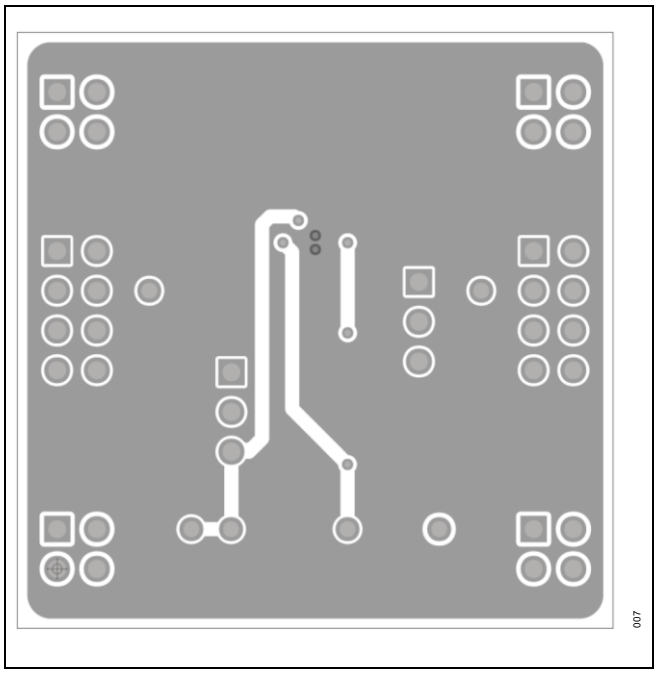
LFCSP Package Evaluation Board PCB Layouts



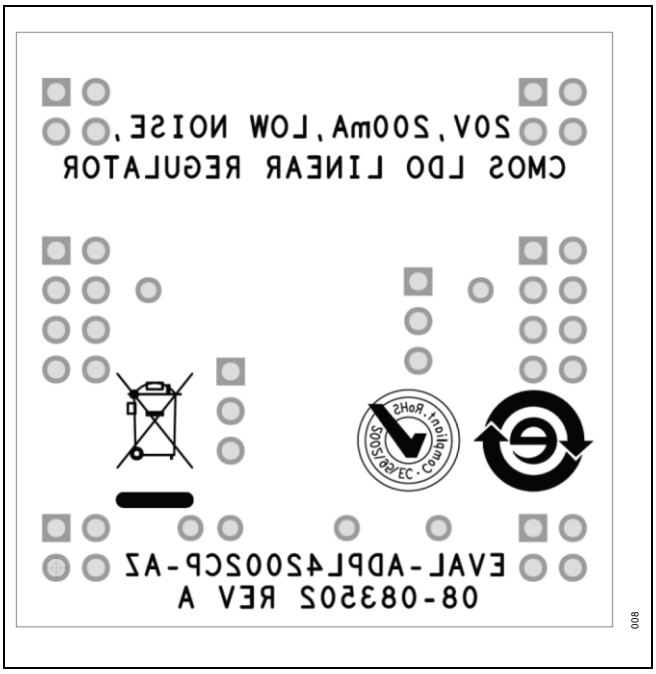
LFCSP Package Evaluation Board—Top Silkscreen



LFCSP Package Evaluation Board—Top

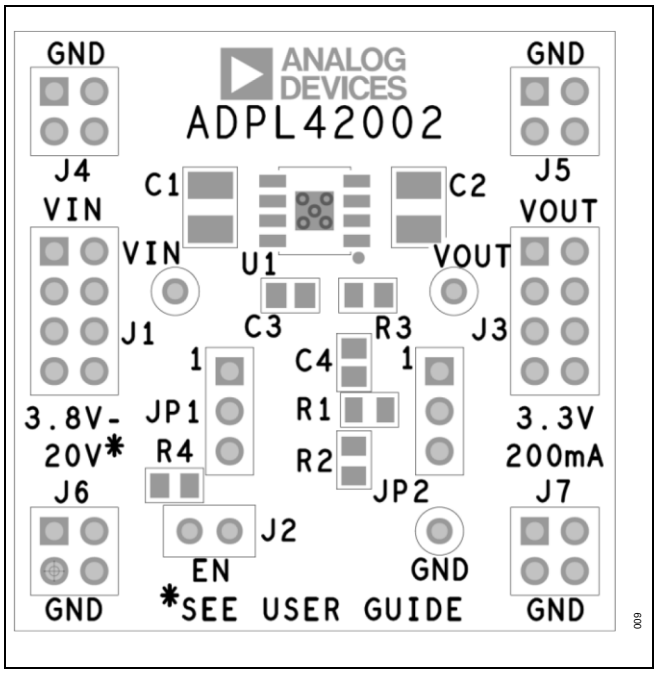


LFCSP Package Evaluation Board—Bottom

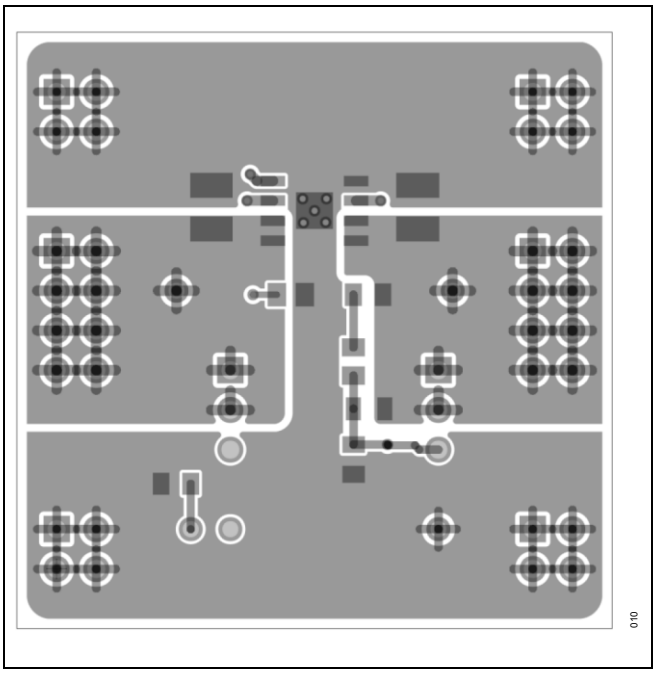


LFCSP Package Evaluation Board—Bottom Silkscreen

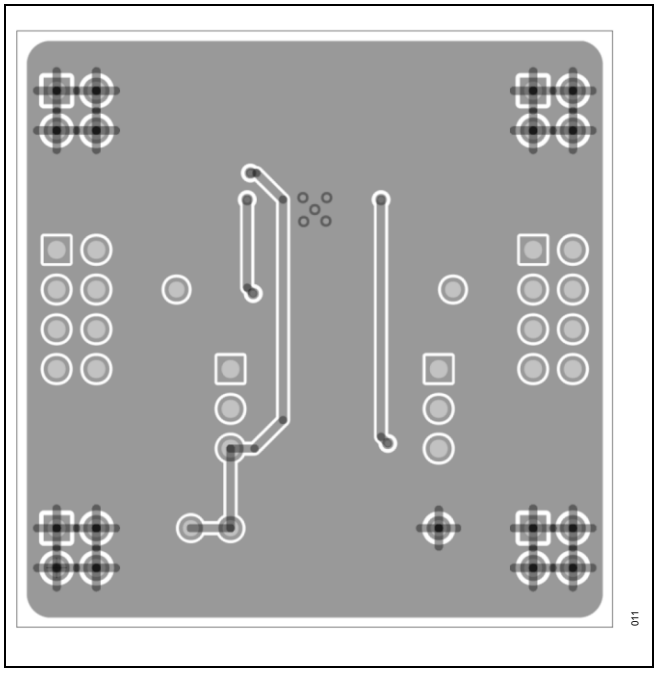
SOIC Package Evaluation Board PCB Layouts



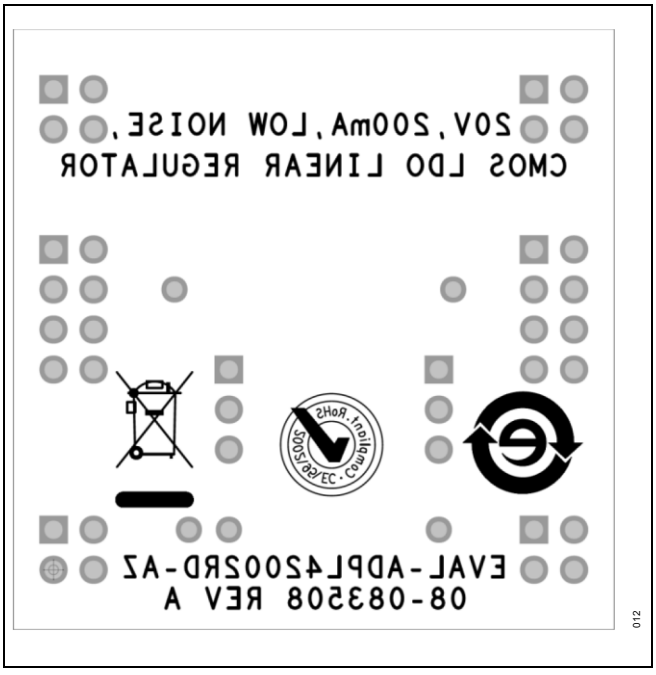
SOIC Package Evaluation Board—Top Silkscreen



SOIC Package Evaluation Board—Top



SOIC Package Evaluation Board—Bottom



SOIC Package Evaluation Board—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/25	Initial release	—

Notes