ADIN3310 Industrial Ethernet TSN Switch Hardware User Guide

FEATURES

- 3 port TSN Ethernet switch in Raspberry Pi Hat footprint
  - All ports RGMII 10Mbps/100Mbps/1000Mbps ADIN1300 PHYs
  - RJ45 with integrated magnetics
  - 2 SFP cages for SGMII copper/fiber connectivity
- Host interface hardware strapping switch, choice of
  - S/D/Q SPI interface or
  - Ethernet port through RJ45 connector
- PHY strapping using surface-mount configuration resistors
  - Default state is auto-neg enabled for all speeds
  - Switch firmware manages PHY operation over MDIO
- Operates from a single, external 5V to 30V supply
- LED indicators on GPIO pins
- IEEE 802.1AS 2020 Time Synchronization
- Time sensitive networking (TSN) capable
  - Scheduled traffic (IEEE 802.1Qbv)
  - Frame preemption (IEEE 802.1Qbu)
  - Per stream filtering and policing (IEEE 802.1Qci)
  - Frame replication and elimination for reliability (IEEE 802.1CB)
- Redundancy capabilities
  - High availability seamless redundancy, HSR
  - Parallel redundancy protocol, PRP
  - Media redundancy protocol, MRP
  - MSTP spanning tree protocol
- NETCONF/YANG configuration using TSN evaluation package or Linux user space driver
- VLAN table control (remapping, reprioritization)
- IGMP snooping
- GPIO/Timer control

EVALUATION KIT CONTENTS

- EVAL-ADIN3310EBZ evaluation board
- 1 USB cable
- 1 Ethernet cable

EQUIPMENT NEEDED

- EVAL-ADIN3310EBZ evaluation kit
- Ethernet cables
- PC running Windows® 10

DOCUMENTS NEEDED

- UG-2280 evaluation board user guide
- UG-2287 software driver user guide
- ADIN3310 data sheet

SOFTWARE NEEDED

- TSN application suite (switch configuration GUI and web server)
- Npcap packet capture

GENERAL DESCRIPTION

This user guide describes how to connect one or more EVAL-ADIN3310EBZ evaluation kits and use the provided software to configure the switch and the TSN features to meet the requirements of a TSN network.

Figure 1 shows an overview of the evaluation board. The evaluation hardware includes the ADIN3310 switch, three ADIN1300 Ethernet PHYs for standard Ethernet connectivity and optional SFP cages for two ports to support SGMII/Fiber modes of operation. The hardware can be powered from a 5V USB cable and is conveniently designed in a Raspberry Pi hat form factor, therefore can easily connect to a RPI for evaluation purposes.

The switch is a managed switch and needs a Host connected for configuration. The TSN switch evaluation application running on a Windows PC can be used to configure the switch for easy evaluation. Alternatively, user can connect own Host over Ethernet or SPI interface.

Full specifications on the ADIN3310 are available in the ADIN3310 data sheet, which is available from Analog Devices, Inc., and must be consulted with this user guide, evaluation board user guide (UG-2280), and software drive user guide (UG-2287) when using the EVAL-ADIN3310EBZ evaluation board.

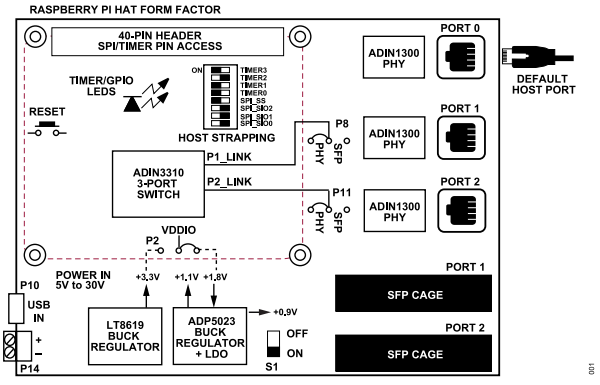

Figure 1. Hardware Overview

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REVISION HISTORY

1/2025—Revision 0: Initial Version

EVALUATION BOARD OVERVIEW

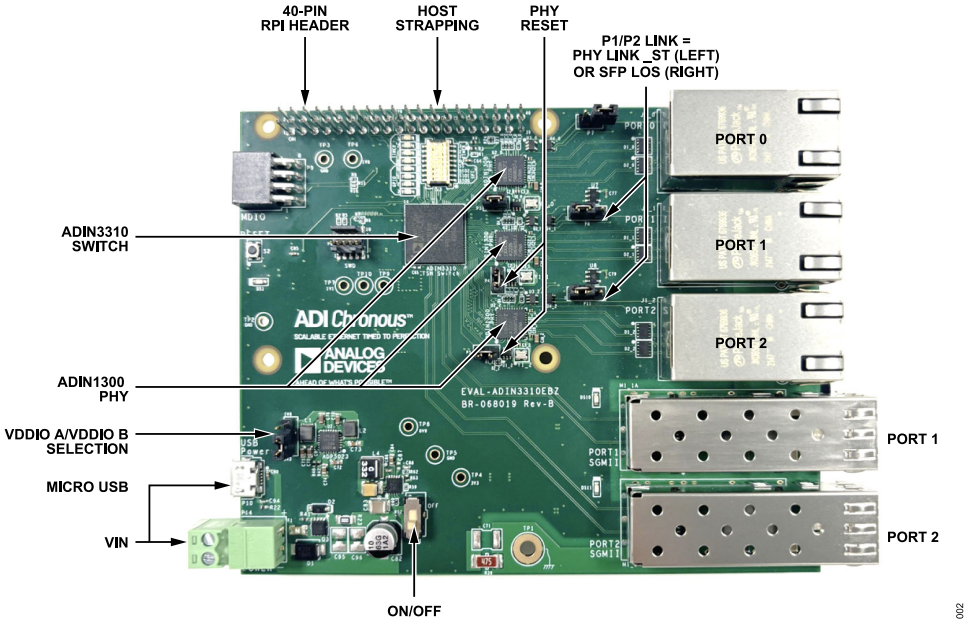

Figure 2. EVAL-ADIN3310EBZ Evaluation Board Overview

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-ADIN3310EBZ operates from a single, external, 5V to 30V supply rail. The power can be applied to a micro USB connector or alternatively to P14 two pin connector. If using the micro USB connector, ensure that the USB port is capable of supplying 500mA current to the board.

When power is applied and S1 switch is turned to ON position, the convertors must generate the required voltage rails and if everything is in sequence, the LED DS1 lights up to indicate a successful power up of the main power rails.

The EVAL-ADIN3310EBZ power requirements are generated from the input power rail by the LT8619 and ADP5023, these generate the four rails required for operation of the ADIN3310 switch and the ADIN1300 Ethernet PHYs along with on-board support circuitry. The default nominal voltages are shown in Table 1.

The default VDDIO of 1.8V is used for both VDDIO_A and VDDIO_B. VDDIO can also be set to 3.3V using jumper P2 (short position 1 and 2).

Table 1. Default Device Power Supply Configuration

Voltage Rail	Nominal Voltage (V)	ADIN3310 Switch	ADIN1300 PHY
VDD3P3_BRD	3.3	VDD3P3	AVDD3P3
VDD1P8_BRD	1.8	VDDIO_A/B	VDDIO
VDD1P1_BRD	1.1	VDDCORE	N/A[1]
VDD0P9_BRD	0.9	N/A[1]	VDD0P9

[1] N/A means not applicable.

Table 2 shows an overview of the EVAL-ADIN3310EBZ current for various operating modes.

Table 2. Board Quiescent Current (P14 = 5V)

Board Status	Typical Quiescent Current
On power-up, Port 0 linked with 1Gbps speed	163mA initially
3 x RGMII, 1000BASE-T	307mA

POWER SEQUENCING

The ADIN3310 device does not have any power supply sequencing requirements, however, the preferred power up sequence is to bring up VDDCORE last and removed first on power down. There are no power sequence requirements for the ADIN1300 devices. The evaluation board is configured to bring up the power rails in the following sequence VDD3P3 and VDD0P9 -> VDDIO_A/B -> VDDCORE.

EVALUATION BOARD OPERATING MODES

The EVAL-ADIN3310EBZ can be used in two general modes. The default use case is with the evaluation package using Port 0 as the Host interface port through the RJ45 connector. Connect Port 0 to a windows PC running the ADI provided TSN evaluation software package for network configuration and control. Port 0 can support both data and control plane traffic, but is not time aware with the PC. In this use case, the other two ports can be used to evaluate all the features of the ADIN3310, establish links with other link partners and evaluate the performance of the chip. UG-2280 shows the TSN evaluation software package and configuration for both the ADIN6310 and ADIN3310.

Alternatively, the user may want to connect their own Host using SPI interface to the switch through the 40-pin connector. Port 0 is now available as a network port and SPI is used for all the control plane configuration of the switch. The Host interacts directly with the TSN driver library in this use case. UG-2287 provides overview of the driver APIs in addition to worked examples.

JUMPER AND SWITCH OPTIONS

The default settings and functions of the jumper options on the board are described in Table 3.

Table 3. Default Jumper, Switch Options and Descriptions

Link	Position	Function
S1	OFF	Power ON/OFF switch.
P2	2-3 Inserted	VDDIO_A = VDDIO_B = 1.8V.
P3	Inserted	Reset signal from switch Port 0 to PHY reset input.
P4	Inserted	Reset signal from switch Port 1 to PHY reset input.
P5	Inserted	Reset signal from switch Port 2 to PHY reset input.
P7	Open	EEPROM WP signal.
P8, P11	1-2 Inserted	Link input to the switch, Px_LINK for Port 1 and Port 2, which support RJ45 or SFP connectivity. The switch expects logic low for link up, high link down. Px_LINK is used to enable the port when driven low. Jumper provides option for link information from the PHY LINK_ST or SFP loss of signal (LOS). Default jumper setting is for PHY to provide link information to switch.

GPIO AND TIMER HEADERS

Timer and GPIO signals are available on P1 connector. When using the ADI TSN evaluation software package, TIMER2 is configured for a 1 pulse per second (1PPS) signal by default and the LED connected to this pin can be observed to blink at a 1 second rate once the board is powered and configured using the evaluation GUI.

ON-BOARD LEDS

The EVAL-ADIN3310EBZ has one LED, DS1, that lights up to indicate a successful power up of the board. There are eight LEDs that are controlled by GPIO (0 to 3) and the Timer (0 to 3) signals.

For the ports that support SFP/fiber interface, (Port 1 and Port 2) there are LEDs (DS10 and DS11) close to the SFP modules, which

EVALUATION BOARD HARDWARE

turn on when an SFP module is inserted and the link is up. The LOS information can be used to drive the switch port Px_LINK input. When using SFP modules, move jumpers P8 and P11 to positions 2 and 3 to route the SFP LOS signal to the switch port Px_LINK input.

STRAPPING AND CONFIGURATION

ADIN3310 Host Port Strapping

The ADIN3310 switch supports stack Processor/Host control over SPI or any of the Ethernet ports. There is no stack processor/microcontroller used on this board, instead for evaluation purposes the TSN switch evaluation application uses a Windows PC as the Host.

When using this hardware, the user can connect an Ethernet Host using any of the Ethernet ports, alternatively, through SPI by connecting to the header P1. In either case, the switch Host strapping must be set for the required Host interface.

The default Host port strapping configuration for this hardware is using Ethernet interface with Port 0 as the Host interface. The switch port is configured for RGMII with no TXC or RXC delays and port speed of 1000Mbps. The link brought up by the PHY on the Host port must match the switch port speed (1000Mbps). In a typical application, a PHY is likely not present in the Host path, instead the port RGMII interface connected directly to the Host MAC interface or SGMII interface to backplane.

The Host port and Host port interface selection are configured using hardware pins, TIMER_0/_1/_2/_3, SPI_SS, and SIOx. By default the SIOx pins have internal pull-down resistors configuring Port 0 as the Host when Ethernet Host is chosen. Table 5 shows the S3 settings required for alternative Host ports.

For more details on all options available, refer to the Host Strapping section on the ADIN3310 data sheet.

Table 4. Host Interface Type Using Switch S3

Interface Type	SPI_SS	TIMER3	TIMER2	TIMER1	TIMER0
Internal PU/PD[1]	PU	PD	PD	PU	PU
SPI (single)	OFF	OFF	OFF	OFF	OFF
SPI (dual)	OFF	ON	OFF	OFF	OFF
SPI (quad) (low drive strength)	ON	OFF	ON	OFF	OFF
SPI (quad) (high drive strength)	ON	ON	ON	OFF	OFF
RGMII 1000M (default)	ON	ON	OFF	ON	ON

[1] PU = pull-up, PD = pull-down.

Table 5. Host Port Using Switch S3

Host Port	SPI_SIO2	SPI_SIO1	SPI_SIO0
Port 0 (default)	OFF	OFF	OFF
Port 1	OFF	OFF	ON
Port 2	OFF	ON	OFF

Host Strapping Switch, S3

DIP switch, S3, provides user ability to change the Host strapping configuration. Figure 3 and Figure 4 show the switch positions required for the default configuration for use with the TSN evaluation application and alternatively for single SPI. Changes to the strapping configuration require a power cycle to take effect.

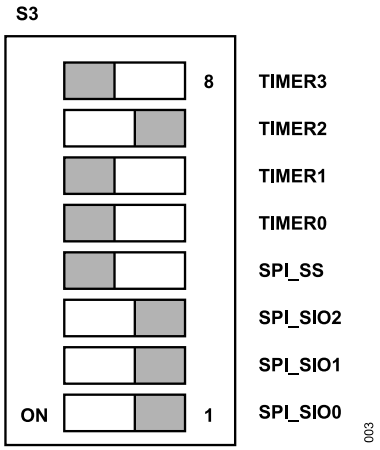

Figure 3. Switch S3 Default Setting for Host Interface Port 0, 1Gbps RGMII no Delays

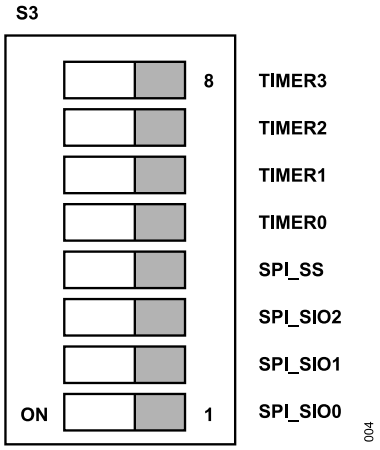

Figure 4. Switch S3 Configuration for Host Interface Using SPI (Single)

ADIN1300 Strapping

There are three ADIN1300 devices on this evaluation board. All three PHYs are configured for auto-neg all speeds. On power up, the PHYs sample their strapping pins and configure themselves accordingly. During switch initialization, the switch interacts with the PHYs and ensures that they are configured appropriately based on the configuration passed from the Host.

ADIN1300 Link Status Polarity

Note that the ADIN1300 LINK_ST pin is by default active high, the evaluation board includes an inverter in the path between the PHY LINK_ST and the Px_LINK input of the switch.

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ADIN1300 PHY Addressing

The ADIN1300 PHY addresses are configured by sampling the RXD pins after power on, when they come out of reset. There is no need for external strapping resistors as the ADIN3310 switch can assign unique PHY addresses to each PHY through default setting of the RXD pins per port. The default PHY addresses assigned to the ADIN1300 devices is shown in Table 6.

Table 6. Default PHY Addressing

Port Number	PHY Address
0	0
1	1
2	2

SWD Interface

This is a debug only port and not available for use.

MDI Interface

The MDI path to the integrated RJ45 includes TVS protection diodes for EMC robustness. The SP337 protection diodes are used here, one pack has four TVS and protects two MDI pairs. The routing of the MDI pairs must be done in such a manner as to not leave any stubs. The footprint of the SP337 leads to a straight-through layout.

SWITCH SOFTWARE

There are two different software packages for use with the switch. The TSN switch evaluation package is provided for ease of evaluation when getting familiar with the switch. When connecting own Host processor to the switch, the TSN driver library provides all the APIs for configuration of the switch.

The following sections summarize each package and how to use with the ADIN3310 switch. Both packages are available to download from the ADIN3310 product page and both packages are common to ADIN6310 and ADIN3310, but the configuration differs depending on the device. The features and capability are the same for the two products, the only difference being the number of ports.

TSN SWITCH EVALUATION PACKAGE

The software package supports configuring the switch for TSN or redundancy capability, which allows user for easily evaluate the device features ahead of developing own prototypes and porting TSN driver library. This software runs on Windows PC, where the GUI application launches a web server, which allows user to configure the switch. In parallel with the web server, a NETCONF server runs on the PC, which enables a user to load switch configurations in YANG module format.

The UG-2280 describes the evaluation package in detail. For description of the software package and getting started, refer to the TSN Switch Evaluation Contents Overview section on the UG-2280.

ADIN3310 CONFIGURATION

Figure 5 shows an overview of the TSN evaluation software package. Before launching the application, first modify the **ses-configuration.txt** file to pass the relevant ADIN3310 XML file. There are a number of XML configuration files already-prepared and located in each file system (FS_SES_InstanceX) for different versions of hardware and different types of configuration. The XML file corresponds to the hardware configuration and tells the switch how user wants it configured. Port configuration must be configured during initial bring-up, similarly, HSR or PRP must be configured initially and cannot be enabled during run-time. All other features can be configured through the web server.

In the **application** folder, navigate and edit the **ses-configuration.txt** file by passing the relevant XML file to the **Startup file name** parameter (see Figure 6). Then launch the application **ADIN6310-tsn-evaluation-util.exe** to start configuring the switch.

The switch does not retain the configuration after a power cycle and, therefore, is required to be configured each time it is powered up.

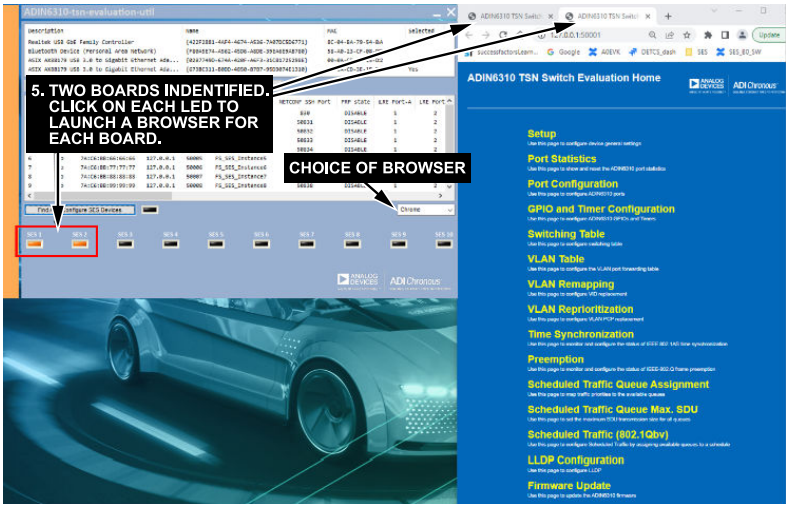

Figure 5. GUI Application and TSN Switch Evaluation − Home Page

SWITCH SOFTWARE

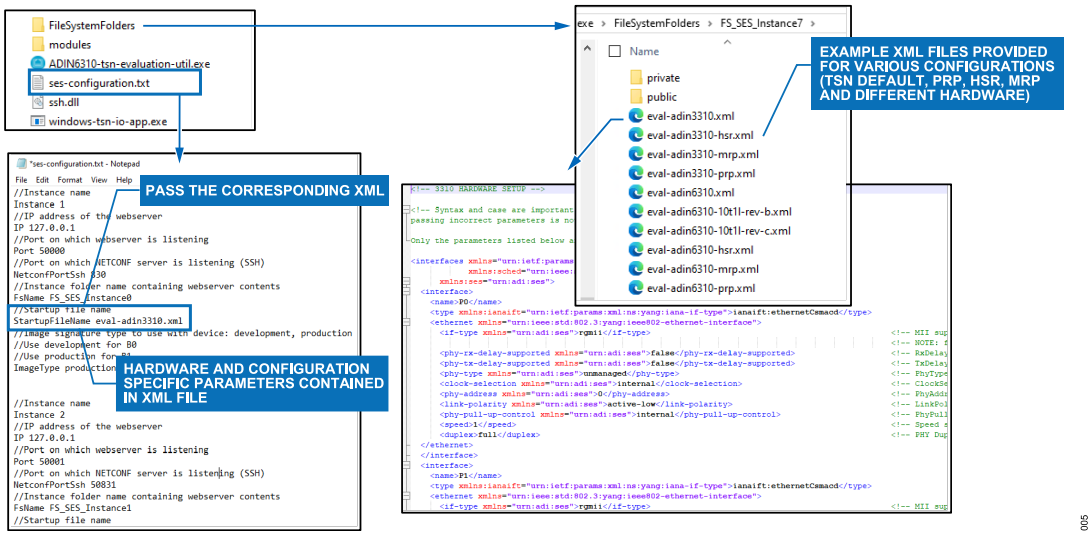

Figure 6. Ses-configuration.txt File Overview and Location of Hardware Configuration XML Files

DIFFERENT XML FILE CONFIGURATIONS

There are a number of XML file examples contained in the FS folder for different switch configurations. The following describes the files relevant to the ADIN3310 device:

- The **eval-adin3310.xml** is intended as a **TSN** configuration and when this file is used, the switch is configured with all ports configured for RGMII mode with Time Synchronization and LLDP enabled. In this mode, all TSN features are available for configuration within the web server.
- The **eval-adin3310-hsr.xml** file configures the switch for HSR mode of operation. Only HSR features are available within the web server when configured for HSR mode. In this mode, VLAN table and LLDP are also supported.
- The **eval-adin3310-mrp.xml** configures the switch for TSN mode of operation with MRP enabled. The MRP configuration, such as MRP mode, which ring ports are defined in the xml file, but can be changed during operation within the web server. All TSN features are available within the web server.
- The **eval-adin3310-prp.xml** configures the switch for PRP mode of operation. Only PRP features are available within the web server when configured for PRP mode.
- The remaining xml files are similar configurations for the ADIN6310 6-port switch and different versions of hardware.

Further configuration can be performed using the web server once the application has successfully identified the device.

Note that passing an ADIN6310 configuration to the ADIN3310 device is rejected as the port counts do not match.

SWITCH SOFTWARE

TSN SWITCH DRIVER LIBRARY

The TSN switch driver package is available as a software download from the ADIN3310 product page. It contains the APIs used for configuration of the switch features. The software is C source code and OS agnostic. This package can be ported to different platforms to interact with the switch and provides access to all the features currently exposed in the switch. Use the driver in conjunction with the UG-2287. When using the driver APIs, the port configuration is specific to the hardware configuration. For this evaluation board, the following snippet of code shows the port initialization structure specifically for this board. This structure is passed to the SES_InitializePorts() API during the initialization of the switch. For more details on the sequence of API calls for the various features, refer to the UG-2287.

```
//{Port enable, MII, RxDelay, txDelay, clk se▶
lection, link polarity, PHY type, {autoneg,
pullupctrl,
phyAddr, Speed, Duplex, Crossover}}
const SES_portInit_t initializePorts_p[] = {
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyA▶
DIN1300, {true, 0, 0, SES_phySpeed1000,
SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyA▶
DIN1300, {true, 0, 1, SES_phySpeed1000,
SES_phyDuplexMode▶
Full, SES_autoMdix}},
{ 1, SES_rgmiiMode, { 0, 0, 0 }, 1, SES_phyA▶
DIN1300, {true, 0, 2, SES_phySpeed1000,
SES_phyDuplexMode▶
Full, SES_autoMdix}}
};
```

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.