DESCRIPTION

Demonstration circuit 804 is a POWER OVER ETHERNET PD INTERFACE WITH INTEGRATED SWITCHING REGULATOR featuring the LTC4267. It provides a complete IEEE 802.3af power device (PD) interface and isolated 3.3V power supply solution for use in Power over Ethernet (PoE) applications.

The LTC4267 integrates the 25kΩ signature resistor, classification current source, thermal overload protection, signature disable and power good signal along with an undervoltage lockout optimized for use with the IEEE required diode bridge. The precision dual level input current limit allows the LTC4267 to charge load capacitors and interface with legacy PoE systems.

The LTC4267 combines the above features with a current mode switching controller designed for driving a 6V rated N-channel MOSFET. It features programmable slope compensation, soft-start, and constant frequency operation, minimizing electrical noise even with light loads.

The DC804 demo board comes in 3 variants, -A, -B and -C, which output 3, 5 and 8.5 watts, respectively. There is also optional circuitry to provide alternative secondary side regulation with the LT4430, a high performance Secondary Side Optocoupler Driver.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Minimum Turn-on Voltage	Input from PSE	-39V
Maximum Turn-off Voltage	Input from PSE	-33V
Auxiliary input voltage range	Input from 24V auxiliary power	+38V to +57V
Minimum operating voltage	I_{out} = Maximum rated load	-36V
Maximum Input Current	Input from PSE	400 mA
Maximum Output Current	Version -A, V_{out}=3.3V	1.0A
	Version -B, V_{out}=3.3V	1.6A
	Version -C, V_{out}=3.3V	2.6A
Output Voltage	V_{in}=48VDC, from PSE, I_{out}=max output current	3.3V, typical
Output Regulation	Line (50% to 100% full load)	±2%, typical
	Load (0% to 100% of rated full load)	±2%, typical
Isolation Voltage	Basic Insulation	250VDC

OPERATING PRINCIPLES

Demonstration circuit 804 interfaces with a customer's Power-Over-Ethernet test setup per Figure 1. The front end of the demo circuit implements the required Ethernet input interface transformer coupling and common-mode termination through the integrated connector J1. The demonstration circuit is setup to allow data to pass in and back out of the board while the DC804 performs IEEE 802.3af interface functions. The Power Sourcing Equipment (PSE) is connected to J1 and the PHY is optionally connected to J2.

The PD is required to have 0.1uF of capacitance during detection and this is provided by C2. It is also required to have at least 5uF of capacitance after the in-rush circuit, provided by capacitors C1 and C9.

This demo circuit allows detection and power classification of the PD per the IEEE 802.3af specification. During the detection process of a PD, the LTC4267 displays the proper 25kΩ signature resistor. Signature detection may be disabled, if so desired, by appropriately setting the jumper at JP5. If signature detection is disabled, all interface functions of the LTC4267 are also disabled. Signature detection, classification, the internal power MOSFET switch and POWER GOOD are all disabled. As this demonstration circuit uses the POWER GOOD signal, the power regulator is disabled, as well.

Classification is programmed by the selection of a single external resistor connected to the RCLASS pin. The classification can easily be set in this demo circuit with the placement of a single jumper on JP0, JP1, JP2, JP3, or JP4.

While every demonstration circuit is equipped with a jumper and the appropriate resistors to select any of the four classes defined as of this printing, not every demonstration circuit can perform as if it were any one of the four classes. That is, DC804A-A is designed to produce 3.3V power for a class 1 PD, DC804A-B for a class 2 device and DC804A-C for a class 3. A DC804A-A, for example, cannot deliver sufficient power for a class 3 device, regardless of the classification jumper position.

After detection and classification, the PD is powered up when the input voltage exceeds the LTC4267 turn-on under-voltage lock out (UVLO) through a dual-level current-limited power switch. While the voltage between POUT and VPORTN is above the Power Good trip point, the amperage through the power switch is held below the low-level current limit. When the voltage between POUT and VPORTN falls below the Power Good trip point, the Power Good signal goes active low and the amperage through the power switch is held below the high-level current limit.

For the PD to remain powered on, it must present to the PSE both AC and DC components of the Maintain Power Signature (MPS). The PD must hold the DC MPS by drawing at least 10mA or the PSE may disconnect power. The DC804 demo circuit can be made to draw the requisite 10mA by enabling the minimum load at JP6.

The synchronous flyback converter operates at a typical switching frequency of 200kHz, controlled by the current mode controller portion of the LT4267. Galvanic isolation is achieved through transformer T1 and opto-isolator ISO2.

The primary side power path is comprised of C1, L1, C9, ½ of T1, Q2, and R11. These components should be as close to each other as possible when laying out the printed circuit board. The components R4 and C6 serve to damp switching spikes on Q2. They should be placed as close as possible to Q2 in order to be effective.

The secondary side power path is made up of the other ½ of T1, D5, C4, C5 and C18. These parts should also be laid out as close to each other as possible, without overlapping any of the circuitry or traces of the primary side. The components R5 and C3 serve to damp switching spikes on D5. They should be placed as close as possible to D5 in order to be effective.

In order to ensure proper operation, the designer must ensure that the PD input current requirement does not exceed the LTC4267 current limit over the unit's operating voltage range.

QUICK START PROCEDURE

Demonstration circuit 804 is easy to set up to evaluate the performance of the LTC4267. For proper equipment setup, refer to the connection diagram and follow the procedure below:

1. With the power source to the PSE turned off, connect the input power supply to the board through the J1 filtered Ethernet connector.
2. In addition to a PSE, the DC804 board can be powered by an alternate input power supply through the VSIG+ and VSIG- terminals. Similarly, the alternate input power supply can be connected through the SPARE+ and SPARE- terminals. Only one set of connections is necessary. Do not connect more than one power source.
3. Install the jumper at one of the locations JP0 through JP4 determine the classification of the power device.
4. Install the jumper at JP5 to "enable."
5. Connect or remove the DC Maintain Power Signature minimum load as desired by appropriately connecting a jumper at JP6.
6. Turn on the PSE or alternate input power supply. Increase the voltage until the power converter turns on. Be careful not to exceed 57VDC. NOTE: Make sure that the input voltage does not exceed 57VDC. If a higher input voltage is required, power components with higher voltage ratings should be used.
7. Verify proper classification, signature detection and Power Good signal status.
8. Check the output voltage. It should be 3.3V, typical. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
9. Once the proper output voltage is established, adjust the load current within the appropriate range and observe the output regulation, ripple voltage, efficiency and other parameters.

The PD interface of the LTC4267 can be bypassed by powering just the DC/DC regulator with an optional auxiliary power source via the V+ and –48V terminals. Even if the PD interface is bypassed, the signature detection must be enabled in order for the POWER GOOD signal to enable the current mode controller.

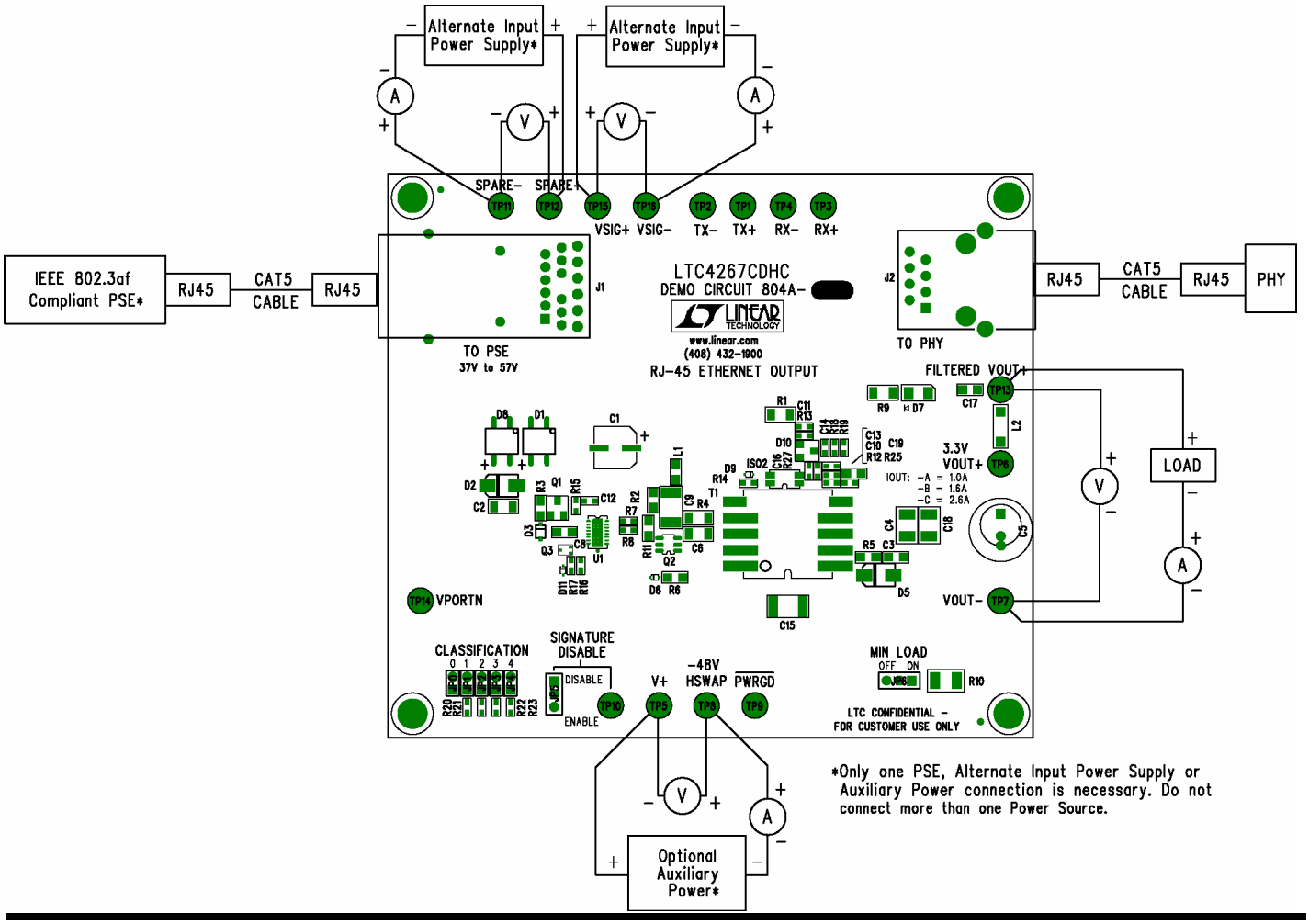
OPTIONAL CIRCUITRY

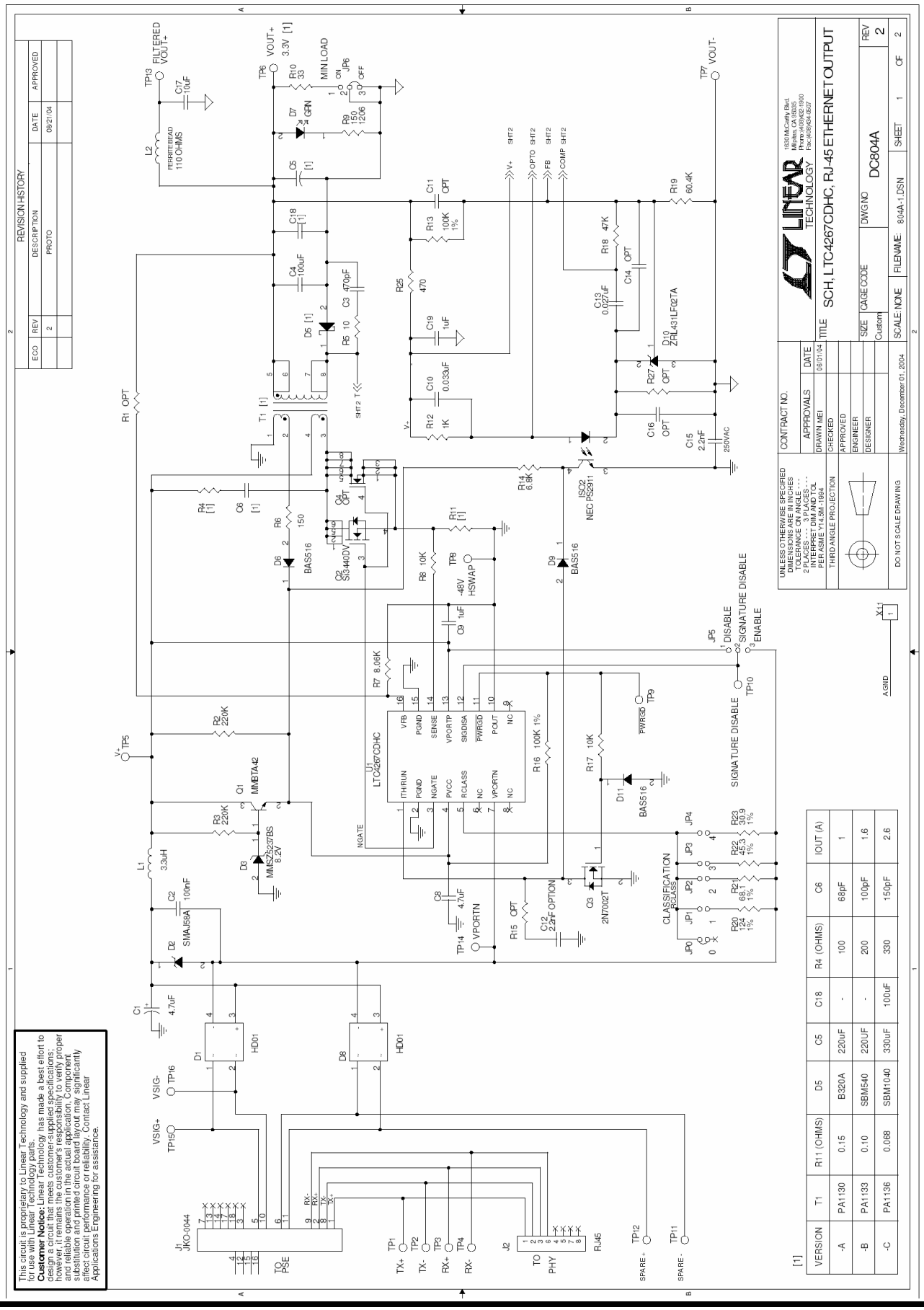
DC804 is equipped with optional circuitry. Their functions fall into three major categories: existing control loop modifications, non-isolated feedback, and LT4430 circuitry.

The pads at locations C11 and C14 are used to modify the existing feedback compensation. The user is cautioned that adding components to these locations will alter the behavior of the voltage regulator, possibly resulting in instability.

The pads located at R1, R15 and C12 are used only if the isolated feedback circuitry is not necessary. In such a case, disable the isolated control circuitry by removing the components at locations D9, ISO2, and R13. Tie the secondary side ground reference to that of the primary by removing C15 and replacing it with a low AC impedance short circuit.

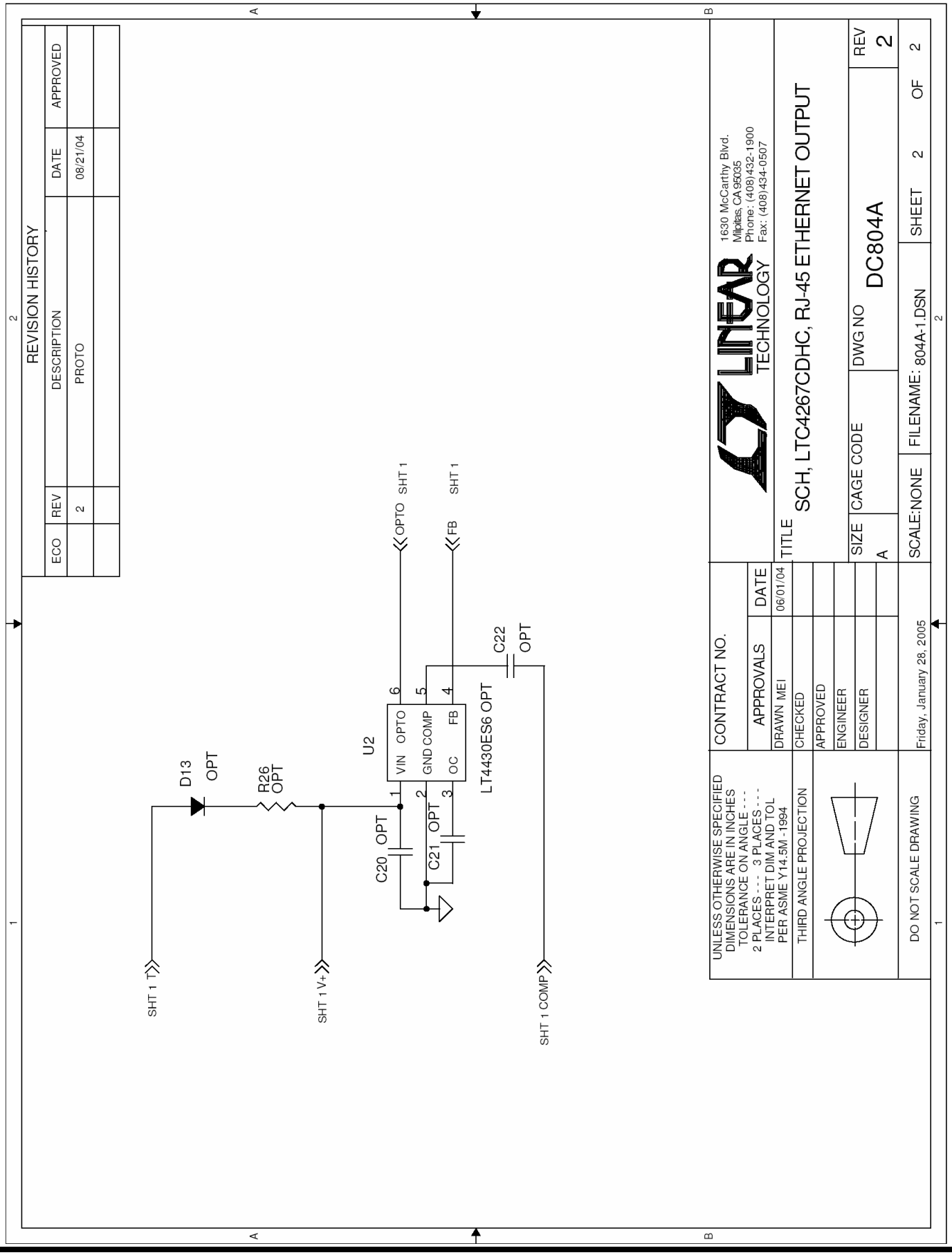
All of the components on the bottom side of the board are used to integrate Linear Technology's LT4430, a high performance secondary side optocoupler driver. The LT4430 features high performance capabilities such as a precision reference, start-up and short circuit recovery overshoot control and high operating bandwidth. To use the LT4430, disable the existing control circuitry by removing R12, C10, R25, C13 and D10, located on the top side, and replace R19 with a 22.1K, 1% resistor. Install the optional components C16, R27, D13, R26, C20, C21, C22 and U2. Please consult the LT4430 data sheet for further details about the proper application of this device.





VERSION	T1	R11 (OHMS)	D5	C5	C18	R4 (OHMS)	C6	IOUT (A)
-A	PA1130	0.15	B320A	220uF	-	100	68pF	1
-B	PA1133	0.10	SBM540	220UF	-	200	100pF	1.6
-C	PA1136	0.068	SBM1040	330uF	100uF	330	150pF	2.6

[1]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REV
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LT4430ES6 OPT
C20 OPT
C21 OPT
C22
OPT
OPTO SHT 1
FB SHT 1
SHT 1 T
SHT 1 V+
SHT 1 COMP
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON ANGLE - - -
2 PLACES - - - 3 PLACES - - -
INTERPRET DIM AND TOL
PER ASME Y14.5M -1994
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS
DATE
DRAWN MEI
06/01/04
CHECKED
APPROVED
ENGINEER
DESIGNER
Friday, January 28, 2005
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
TITLE
SCH, LTC4267CDHC, RJ-45 ETHERNET OUTPUT
SIZE
A
CAGE CODE
DWG NO
DC804A
REV
2
SCALE:NONE
FILENAME: 804A-1.DSN
SHEET 2 OF 2