# DESCRIPTION

Demonstration circuit 699 supports a family of 12/14-Bit 80 MSPS ADCs. Each assembly features one of the following devices: LTC1749 or LTC1750 high speed, high dynamic range ADCs.

Two versions of the DC699 demo board support the LTC1749 and LTC1750 A/D converters and are listed in Table 1. Depending on the required resolution the DC699 is supplied with the appropriate A/D.

**Design files for this circuit board are available. Call the LTC factory.**

**Table 1. DC699 Variants**

| DC699 VARIANTS | ADC PART NUMBER | RESOLUTION | MAXIMUM SAMPLE RATE | INPUT FREQUENCY |
|---|---|---|---|---|
| 699A-A | LTC1749 | 12-Bit | 80Msps | Ain < 500MHz |
| 699A-B | LTC1750 | 14-Bit | 80Msps | Ain < 500MHz |

**Table 2. Performance Summary ($T_A$ = 25°C)**

| PARAMETER | CONDITION | VALUE |
|---|---|---|
| Minimum Supply Voltage | Depending on sampling rate and the A/D converter provided, this supply must provide up to 400mA. | 4.75V |
| Maximum Supply Voltage | | 5.25V |
| Analog input range | Depending on Sense and PGA Pin Voltages | 0.84, 1.35, 1.4 or 2.25VP-P |
| Logic Input Voltages | Minimum Logic High | 2.4V |
| | Maximum Logic Low | 0.8V |
| Logic Output Voltage (74VCX16373 output buffer) | Minimum Logic High @ +12mA | 2.0V |
| | Maximum Logic Low @ -12mA | 0.4V |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 | |
| Encode Clock Level | 50 Ohm Source Impedance, AC coupled or ground referenced (Encode Clock input is transformer coupled on board.) | $2V_{P-P}$ Sine Wave |
| Resolution | See Table 1 | |
| Input frequency range | See Table 1 | |
| SFDR | See Applicable Data Sheet | |
| SNR | See Applicable Data Sheet | |

# QUICK START PROCEDURE

Demonstration circuit 699 is easy to set up to evaluate the performance of the LTC1749/LTC1750 family of A/D converters. These devices are related to the LTC1748 and other family members but are optimized

for under-sampling applications extending from frequencies in the region of the sample rate, to 500 MHz.

## SETUP

If a DC718 QuickEval-II Data Acquisition and Test System was supplied with the DC699 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC699 and to a PC running Windows98, 2000 or XP.

Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

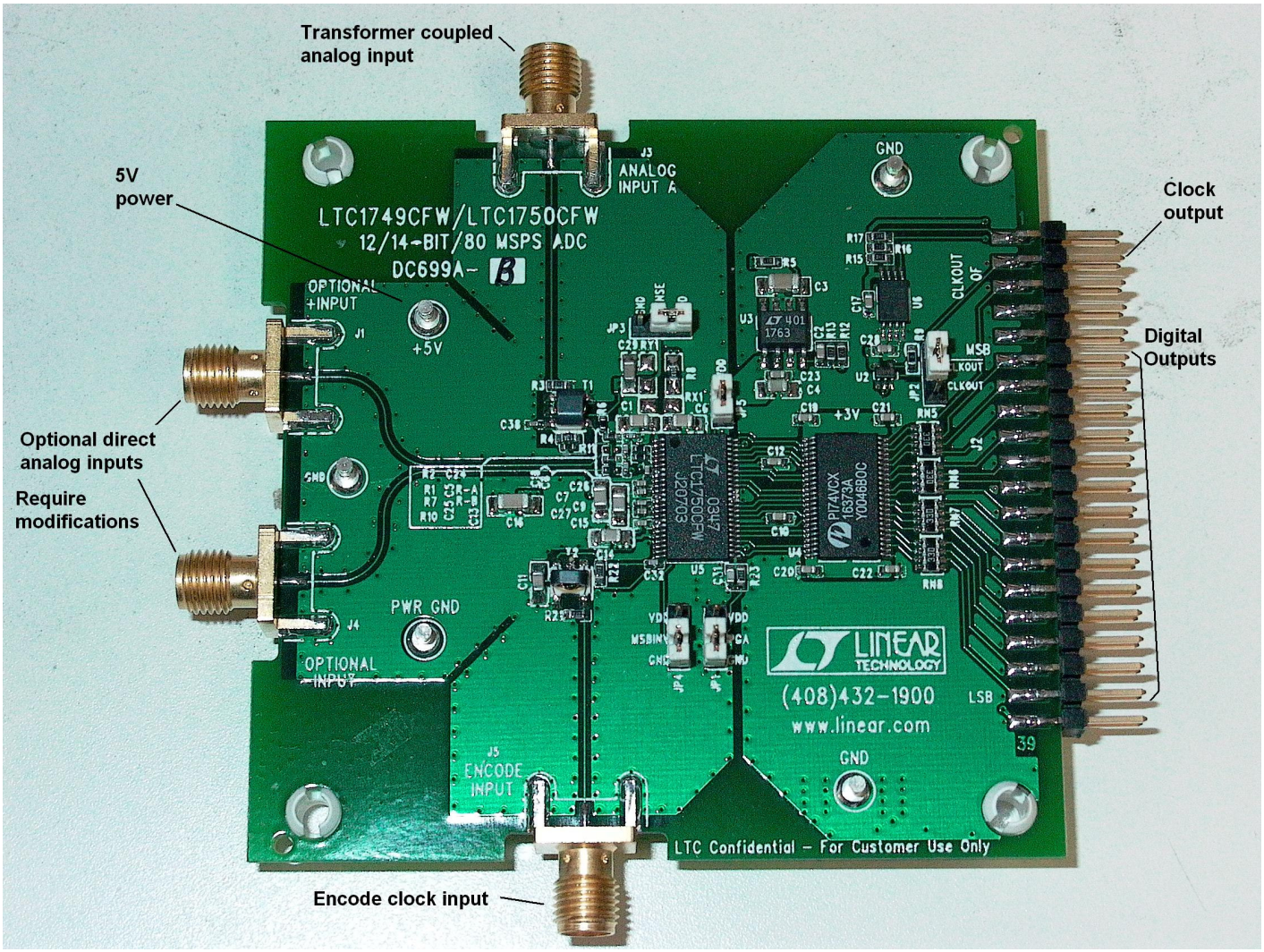



**Figure 1. DC699 Setup**

## DC699 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC699 demonstration circuit board should have the following jumper settings as an initial start condition:

JP1: PGA to ground Input range ± REF

PGA to VDD Input range ± REF/1.6666

JP2: Set to CLKOUT (not CLKOUT bar for QuickEval-II compatibility.)

JP3: SENSE to GND selects 0.70V reference
SENSE to VDD selects 1.125V reference

JP4: Connect MSBINV to GND (For 2's compliment output format for PScope compatibility.)

JP5: Connects OVDD to ADC (remove for experimentation)

## APPLYING POWER AND SIGNALS TO THE DC699 DEMONSTRATION CIRCUIT BOARD:

If a DC718 is used to acquire data from the DC699, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +5V across the pins marked "+5V" and "PWR GND" on the DC699. The DC699 demonstration circuit requires up to 400 mA depending on sampling rate and A/D converter supplied.

The data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub in which case it must be supplied an external 6-9V on turrets G7(+) and G1(-) or the adjacent power jack.

## ENCODE CLOCK

**NOTE: THIS IS NOT A LOGIC LEVEL INPUT**. Apply an encode clock to the SMA connector on the DC699 demonstration circuit board marked "ENCODE INPUT". Refer to Table 2 for recommended level, impedance and coupling. Do not connect to a signal source with a DC offset. This input is connected to ground through the primary of transformer T2. For the very best noise performance, the ENCODE INPUT must be driven with a very low jitter clock source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $2V_{P-P}$. Using band pass filters on the clock and the analog input will improve the noise performance.

[Data Sheet FFT plots are taken using 10 Pole TTE band pass filters on both the encode clock and analog signal sources which are generated by low phase noise Agilent 8664B signal generators.]

Apply the analog input signal of interest to the SMA connector on the DC699 demonstration circuit board marked "ANALOG INPUT A". Do not connect to a signal source with a DC offset. This input is connected to ground through the primary of transformer T1. Optional direct differential inputs are provided via J1 and J4. To use the optional differential inputs requires removing and adding several components on the DC699. Refer to the DC699 schematic for further information.

At this point a conversion clock output is available on pin 3 of J2 and data samples are available on Pins 11-37 for 14 BITS or (15-37 for 12 BITS) which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40 pin ribbon cable or collected by the DC718 QuickEval-II using the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC699 demonstration circuit by selecting the correct

A/D Converter as installed on the DC699. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, either LTC1749 or LTC1750.

If everything is hooked up properly, powered and a suitable convert clock and analog inputs are present, pressing the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

## ANALOG INPUT NETWORK

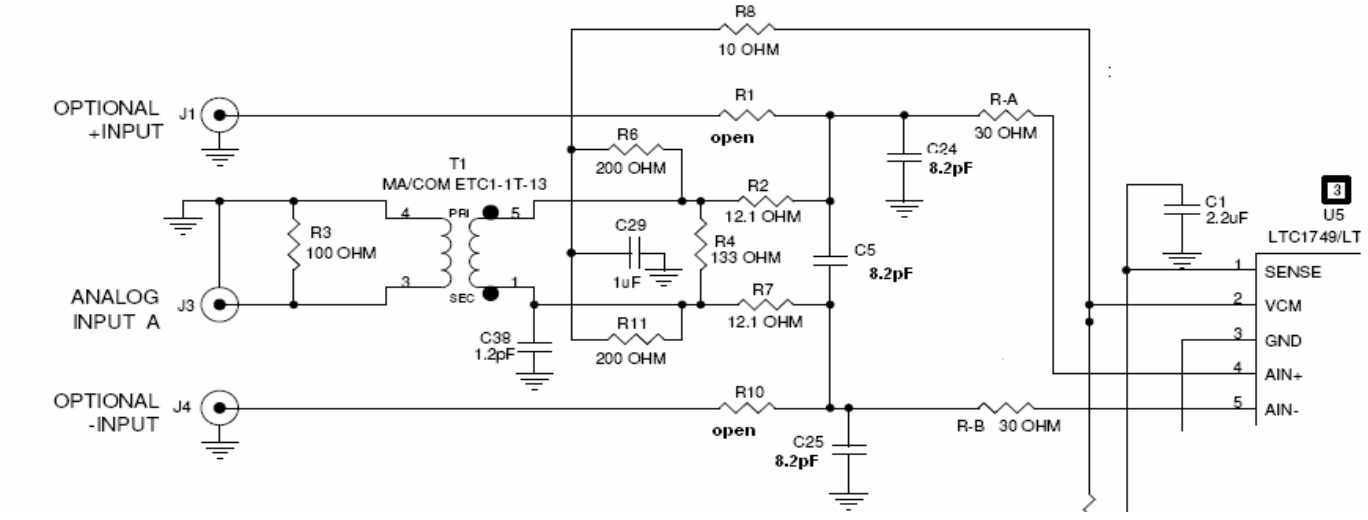
These ADCs are related to other members of the LTC174x family (demo board DC520), however the LTC1749 and LTC1750 are optimized for under-sampling. For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for the analog input frequency to the ADC. For input frequencies above 80 MHz, the circuit in Fig. 2 is recommended. This is the circuit as configured for this demo board and uses a different transformer than the DC520 (T1-1T).

The transformer supplied may not produce good results below 20 MHz. The LTC1749 and LTC1750 can be used in these lower frequency ranges if the customer desires to use a single part number for both over-sampling and under-sampling applications. Capacitors C5, C24 and C25 can be changed to 12 pF for 40-80 MHz, and to 22 pF below 40 MHz. These recommendations are assuming a 50Ω signal source. For direct DC drive, R2 and R7 should be removed, and similar values installed in positions R1 and R10.

If a very low noise driver such as an AH3 or AH22 from WJ communications is used, the capacitors C5, C24 and C25 can be quite low in value without raising the noise floor. For frequencies above 200 MHz, it may be desirable to replace the RC band limiting filter with a balanced Pi low pass impedance matching circuit. For example, replace R4 with a capacitor (10-20 pF), R2 and R7 can be replaced with single layer inductors in the range of 6-40 nH, C24 an C25 in the range of 2-3 pF, and C5 in the range of 6-10pF. R-A and R-B can be reduced to the range of 10-20 ohms.

Please contact the Linear Technology Applications Department if you would like a DC699 demonstration circuit board with other circuits installed, or for recommendations for specific frequencies and bandwidths.

**Figure 2. Analog Front End Circuit For $A_{IN}$ > 40MHz**



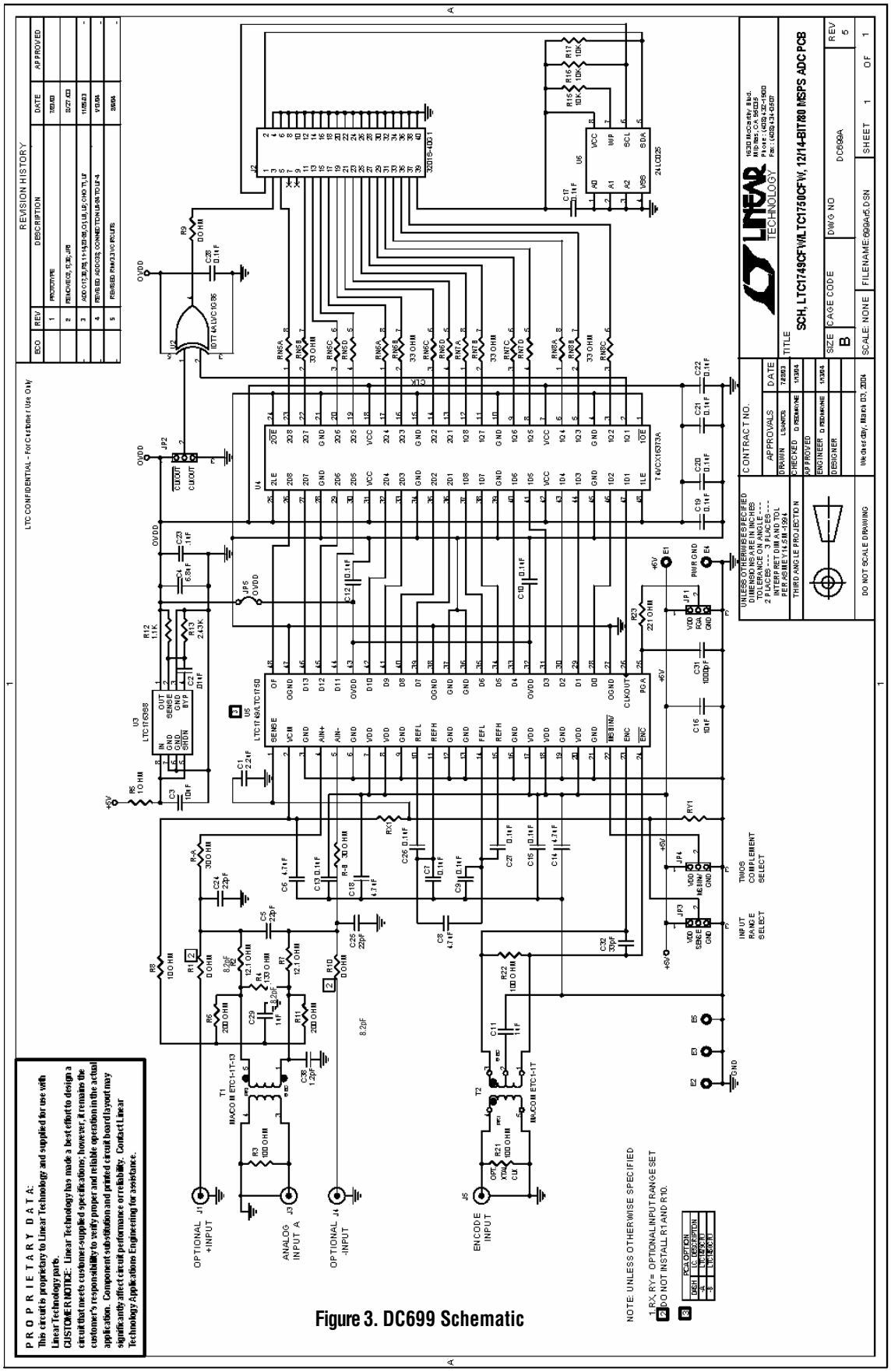



**Figure 3. DC699 Schematic**