MAX16193B/C:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

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1 | Overview

The scope of this document is to provide a report on MAX16193B/C to support in functional safety designs. This contains:

- Failure-In-Time (FIT) rates of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX16193 is a highly accurate, dual-channel supervisor circuit that monitors system supply rails for undervoltage and overvoltage faults. It has two input channels, both with ±*0.3% accuracy*.

The device offers various factory-set thresholds and features two independent, active-low reset outputs available in open-drain (MAX16193B) or push-pull (MAX16193C) versions. These outputs assert low when the monitored voltage rail is out of range and deassert after a set timeout when the voltage normalizes. The MAX16193 comes in a compact package suitable for industrial applications, operating from -40°C to +125°C.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX16193B/C	Dual-Channel Supervisory Circuit	Monitor if a System Supply Voltage is out-of-range (UV/OV) and Assert RESET for a minimum reset timeout period

Figure 1-1 shows the product specific block diagram of MAX16193B/C.

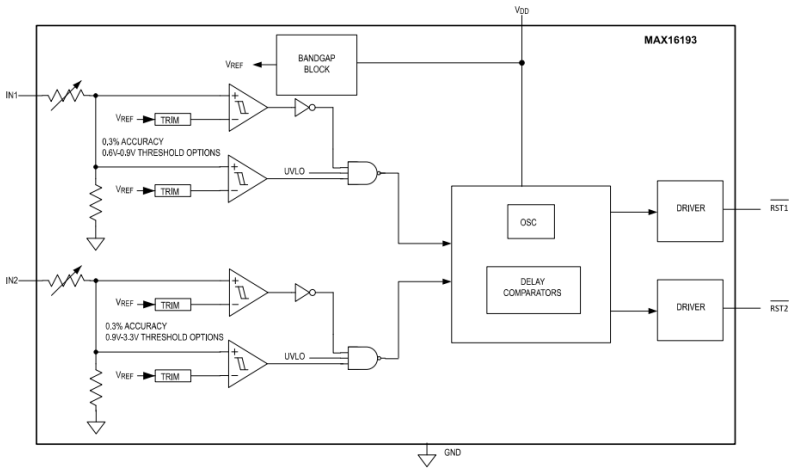

Figure 1-1 MAX16193B/C Block Diagram

MAX16193B/C was developed following a quality-managed development process in compliance with ISO 9001 quality management system standards but was not developed in compliance with IEC61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT) Rates

This section offers specific details on the base functional safety failure-in-time (FIT) rates for MAX16193B/C, according to SN29500, IEC 62380 and accelerated testing conditions of HTOL. It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT rates according to SN29500
- Table 2-2 provides FIT rates according to IEC 62380
- Table 2-3 provides FIT rates according to HTOL

The FIT rates of MAX16193B/C based on SN29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT Rate According to SN29500

SN29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT Rate	50.07

- Mission Profile: 20 years constant operation at 55°C temperature
- Climate type: World-wide (Table 8)
- Operating Voltage (max): 5.5V
- Power Dissipation: 0.5mW
- Theta-JA: 60°C/W
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT
- Part is sensitive to drift

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on SN29500.

- SN29500 part and section: Part 2/Section 5 and ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 5k-50k

The FIT rates of MAX16193B/C based on IEC62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT Rates According to IEC62380

IEC62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4.66
Die FIT Rate	4.28
Package FIT Rate	0.38

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on IEC62380.

- FIT rate calculation model: Section 7.3.1, refer to Mathematical Model
- IEC62380 part and section for die FIT rate: Table 16, MOS ASIC circuits, Full Custom
- Production year for die FIT rate: 2022
- Integration Density: 5k-50k
- IEC62380 part and section for package FIT rate: Table 17b, Peripheral Connection Packages
- Package type: TDFN 8 pins, length: 3mm, width: 2mm, pitch: 0.5mm
- Interface device (EOS relevant): No

The FIT rates of MAX16193B/C based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT Rates According to HTOL Test

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	0.31
90%	0.59
95%	0.76
99%	1.17

Note 3: The FIT rates for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 73,527
- Number of Failures: 0
- Activation Energy: 0.7eV
- Raw Device Hours: 51,021,564
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 3,928,815,128

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for MAX16193B/C as derived from the component die area ratio and complexity, and from engineering expertise.

Since some failures had no effect and do not contribute to any failure mode, the total percentage of the Failure Mode Distribution would not add up to 100%. A Correction factor (CF) was applied to the distribution to account for failures with no effect on the system.

System Function

- Monitor if a System Supply Voltage is out-of-range (UV/OV) and Assert RESET for a minimum reset timeout period

Table 3-1 Failure Mode Distribution (CF = 1.035)

Failure Modes	Failure Mode Distribution
Part stuck with reset output asserted	33%
Part never asserts reset	35%
Part does not detect UV	8%
Part does not detect OV	6%
RESET triggered too early	10%
RESET triggered too late	8%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX16193B/C. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX16193B/C. Refer to the product datasheet for a detailed description of each pin's function.

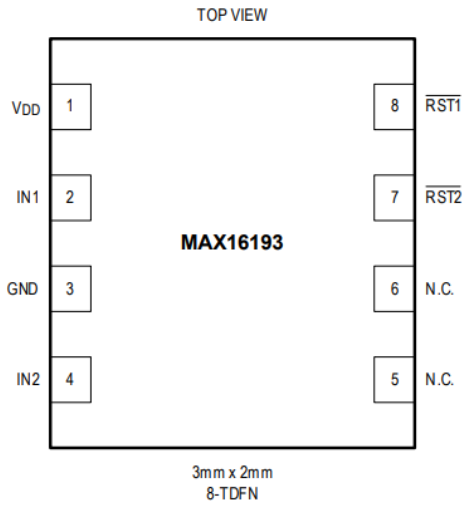

Figure 4-1. MAX16193B/C Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA, based on the Typical Application Circuit, unless otherwise noted:

- The $\overline{RST1}$ and $\overline{RST2}$ pins are active-low reset output available in either open-drain or push-pull configuration.
- In the open-drain version, the $\overline{RST1}$ and $\overline{RST2}$ pins are connected to a 10kΩ pull-up resistor.
- The operating voltage range (VDD) is from 1.7V to 5.5V, and the operating temperature range (T_A=T_J) is from -40°C to +125°C.
- Typical values are measured at VDD = 3.3V, VIN1 = 0.9V, VIN2 = 3.280V, and T_A = +25°C.

Table 4-1 Pin FMEA for MAX16193B/C Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	No effect
2	IN1	OV on Input 1 is triggered
3	GND	Part not functional.
4	IN2	OV on Input 2 is triggered
5	NC	No effect
6	NC	No effect
7	$\overline{\text{RST2}}$	$\overline{\text{RST2}}$ is always high
8	$\overline{\text{RST1}}$	$\overline{\text{RST1}}$ is always high

Table 4-2 Pin FMEA for MAX16193B/C Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	Part not functional.
2	IN1	UV on Input 1 is triggered
3	GND	No effect
4	IN2	UV on Input 2 is triggered
5	NC	No effect
6	NC	No effect
7	$\overline{\text{RST2}}$	System stays falsely reset
8	$\overline{\text{RST1}}$	System stays falsely reset

Table 4-3 Pin FMEA for MAX16193B/C Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	Part is non-functional/Off
2	IN1	UV on Input 1 is triggered
3	GND	$\overline{\text{RST}}$ is inactive/non-functional
4	IN2	UV on Input 2 is triggered
5	NC	No effect
6	NC	No effect
7	$\overline{\text{RST2}}$	$\overline{\text{RST2}}$ has unreliable output
8	$\overline{\text{RST1}}$	$\overline{\text{RST1}}$ has unreliable output

Table 4-4 Pin FMEA for MAX16193B/C Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	VDD	IN1	OV on Input 1 is triggered
2	IN1	GND	UV on Input 1 is triggered
3	GND	IN2	UV on Input 2 is triggered
4	IN2	NC[1]	No effect
5	NC	NC[2]	No effect
6	NC	$\overline{\text{RST2}}$	No effect
7	$\overline{\text{RST2}}$	$\overline{\text{RST1}}$	OR-ing reset behavior
8	$\overline{\text{RST1}}$	VDD	$\overline{\text{RST1}}$ is always high

[1]NC refers to pin 5.
[2]NC refers to pin 6.

5 | Revision History

Revision	Revision Date	Description
A	August 2024	Initial Release
B	September 2024	Updated Document Title, Formatting, Failure Mode Distribution

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

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