MAX16128:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

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Contents

1 | Overview

The scope of this document is to provide a report on MAX16128 to support in functional safety designs. This contains:

- Failure-In-Time (FIT) rates of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX16128 is a load-dump/reverse-voltage protection circuit designed to safeguard power supplies from damaging input voltage conditions. This device can handle input voltages from -36V to +90V and can operate down to +3V. The device uses a fixed overvoltage (OV) and undervoltage (UV) thresholds minimizing external component count.

Key features of this device include flag output indicating fault conditions, and built-in thermal protection. The MAX16128 provides a switch-mode fault management for overvoltage and thermal-shutdown conditions. It is available in an 8-pin µMAX® package. MAX16128 operates over the extended temperature range of -40°C to +125°C.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX16128	Load-dump/reverse-voltage protection circuit	Detect input fault conditions and pull the gate output low to turn off the switch and asserts $\overline{\text{FLAG}}$ when an overvoltage, undervoltage, overtemperature, or output voltage (VOUT) < 90% of input voltage (VIN) fault occurs.

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Figure 1-1 shows the product specific block diagram of MAX16128.

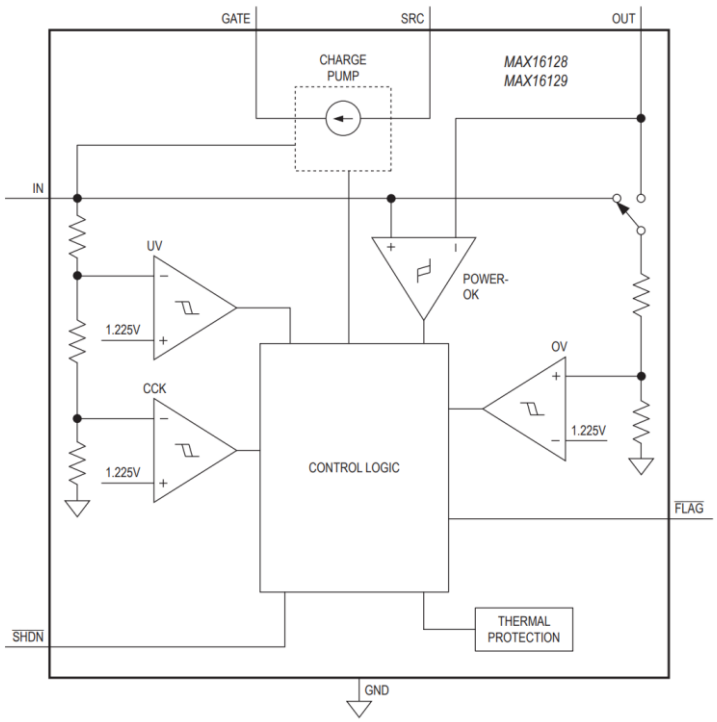

Figure 1-1 MAX16128 Block Diagram

MAX16128 was developed following a quality-managed development process in compliance with ISO 9001 quality management system standards but was not developed in compliance with IEC61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT) Rates

This section offers specific details on the base functional safety failure-in-time (FIT) rates for MAX16128, according to SN29500, IEC 62380 and accelerated testing conditions of HTOL. It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT rates according to SN29500
- Table 2-2 provides FIT rates according to IEC 62380
- Table 2-3 provides FIT rates according to HTOL

The FIT rates of MAX16128 based on SN29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT Rate According to SN29500

SN29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT Rate	39.76

- Mission Profile: 20 years constant operation at 55°C temperature
- Climate type: World-wide (Table 8)
- Operating Voltage (max): 30V
- Power Dissipation: 12mW
- Theta-JA: 77.6°C/W
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT
- Part is sensitive to drift

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on SN29500.

- SN29500 part and section: Part 2/Section 5 and ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 5k-50k

The FIT rates of MAX16128 based on IEC62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT Rates According to IEC62380

IEC62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5.28
Die FIT Rate	5.03
Package FIT Rate	0.25

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on IEC62380.

- FIT rate calculation model: Section 7.3.1, refer to Mathematical Model
- IEC62380 part and section for die FIT rate: Table 16, MOS ASIC circuits, Full Custom
- Production year for die FIT rate: 2011
- Integration Density: 5k-50k
- IEC62380 part and section for package FIT rate: Table 17b, Two rows connections packages
- Package type: µMAX® 8 pins, length: 3mm, width: 3mm, pitch: 0.65mm
- Interface device (EOS relevant): No

The FIT rates of MAX16128 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT Rates According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	1.16
90%	2.21
95%	2.87
99%	4.42

Note 3: The FIT rates for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 15,353
- Number of Failures: 0
- Activation Energy: 0.7eV
- Raw Device Hours: 13,516,848
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 1,040,838,280

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for MAX16128 as derived from the component die area ratio and complexity, and from engineering expertise.

Since some failures had no effect and do not contribute to any failure mode, the total percentage of the Failure Mode Distribution would not add up to 100%. A Correction factor (CF) was applied to the distribution to account for failures with no effect on the system.

System Function

- Detect input fault conditions and pull the gate output low to turn off the switch and asserts $\overline{\text{FLAG}}$ when an overvoltage, undervoltage, overtemperature, or output voltage (VOUT) < 90% of input voltage (VIN) fault occurs.

Table 3-1 Failure Mode Distribution (CF = 1.06)

Failure Modes	Failure Mode Distribution
Cannot pull GATE pin low to turn OFF switch	18%
Cannot pull GATE pin up to turn ON switch	40%
GATE output pulled low early	5%
GATE output pulled low late	5%
$\overline{\text{FLAG}}$ always asserted	7%
$\overline{\text{FLAG}}$ never asserted	15%
$\overline{\text{FLAG}}$ asserted early	5%
$\overline{\text{FLAG}}$ asserted late	5%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX16128. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX16128. Refer to the product datasheet for a detailed description of each pin's function.

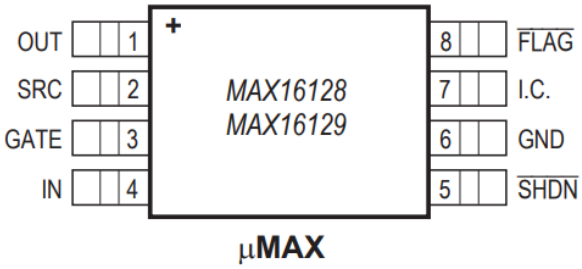

Figure 4-1. MAX16128 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA, based on the Typical Application Circuit, unless otherwise noted:

- The operating voltage range (V_{IN}) is from 3V to 30V, and the operating temperature range (TA) is from -40°C to +125°C.

Table 4-1 Pin FMEA for MAX16128 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	OUT	No fault detection on POK. $\overline{\text{FLAG}}$ stuck high. Part will not pull down GATE pin
2	SRC	Part can still control external switch but external switch VGS may exceed rating
3	GATE	GATE stuck at supply. Switches are always "weakly ON"
4	IN	No effect
5	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low but system can still detect faults. Part can get damaged on $\overline{\text{SHDN}}$ forced low
6	GND	Part not functional
7	I.C.	Input shorted to GND. Part not functional
8	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ stuck high

Table 4-2 Pin FMEA for MAX16128 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	OUT	POK always low. $\overline{\text{FLAG}}$ always low. GATE always low
2	SRC	Part can still control external switch but VIN will be shorted to GND through external switch
3	GATE	GATE stuck at low. Cannot turn on external switch
4	IN	Input shorted to GND. Part not functional
5	$\overline{\text{SHDN}}$	$\overline{\text{FLAG}}$ stuck low. GATE voltage always GND
6	GND	No effect
7	I.C.	No effect
8	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ always low

Table 4-3 Pin FMEA for MAX16128 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	OUT	POK always low. $\overline{\text{FLAG}}$ always low. GATE always low
2	SRC	No effect
3	GATE	GATE pin unconnected. Cannot turn on external switch
4	IN	Part has no power. Part is non-functional
5	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low, but system can still detect faults
6	GND	Part not functional
7	I.C.	No effect
8	$\overline{\text{FLAG}}$	Unreliable $\overline{\text{FLAG}}$ output

Table 4-4 Pin FMEA for MAX16128 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	OUT	SRC	Damage on reverse voltage. Part not functional
2	SRC	GATE	GATE pin voltage won't go above SRC voltage. Cannot turn on external switch
3	GATE	IN	GATE stuck at supply. Switches are always "weakly ON"
4	IN	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low, but system can still detect faults. Part can get damaged on $\overline{\text{SHDN}}$ forced low
5	$\overline{\text{SHDN}}$	GND	$\overline{\text{FLAG}}$ stuck low. GATE voltage always GND
6	GND	I.C.	No effect
7	I.C.	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ always low
8	$\overline{\text{FLAG}}$	OUT	$\overline{\text{FLAG}}$ stuck high

5 | Revision History

Revision	Revision Date	Description
A	October 2024	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

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