MAX16059:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

OCTOBER 2024

Contents

1 | Overview

The scope of this document is to provide a report on MAX16059 to support in functional safety designs. This contains:

- Failure-In-Time (FIT) rates of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX16059 is an ultra-low-current 125nA (typ) microprocessor (µP) supervisory circuit that monitors single system supply voltage. When the VCC supply voltage drops below the factory-trimmed reset threshold level (available from 1.575V to 4.625V in approximately 100mV increments) or manual reset is pulled-low, it asserts an active-low reset signal. This reset signal remains asserted for an externally adjustable reset timeout period after the voltage rises above the reset threshold.

The device offers open-drain output configuration and operates in an extended temperature range from -40°C to +125°C and comes in a compact 6-pin TDFN package.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX16059	Ultra-low-current supervisory circuit	Assert $\overline{\text{RESET}}$ when supply undervoltage (UV) fault is detected

Figure 1-1 shows the product specific block diagram of MAX16059.

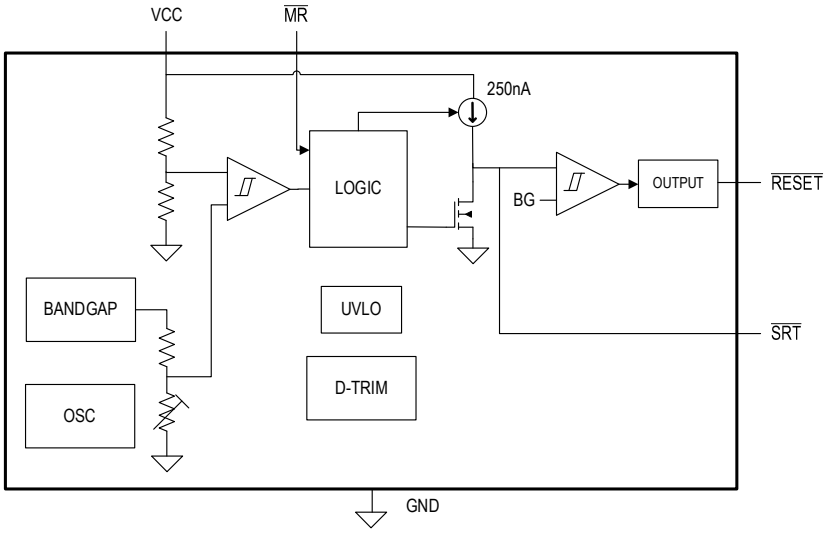

Figure 1-1 MAX16059 Block Diagram

MAX16059 was developed following a quality-managed development process in compliance with ISO 9001 quality management system standards but was not developed in compliance with IEC61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT) Rates

This section offers specific details on the base functional safety failure-in-time (FIT) rates for MAX16059, according to SN29500, IEC 62380 and accelerated testing conditions of HTOL. It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT rates according to SN29500
- Table 2-2 provides FIT rates according to IEC 62380
- Table 2-3 provides FIT rates according to HTOL

The FIT rates of MAX16059 based on SN29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT Rate According to SN29500

SN29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT Rate	40.01

- Mission Profile: 20 years constant operation at 55°C temperature
- Climate type: World-wide (Table 8)
- Operating Voltage (max): 5.5V
- Power Dissipation: 82.5µW
- Theta-JA: 42°C/W
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT
- Part is sensitive to drift

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on SN29500.

- SN29500 part and section: Part 2/Section 5 and ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 50-5k

The FIT rates of MAX16059 based on IEC62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT Rates According to IEC62380

IEC62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5.52
Die FIT Rate	5.14
Package FIT Rate	0.38

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on IEC62380.

- FIT rate calculation model: Section 7.3.1, refer to Mathematical Model
- IEC62380 part and section for die FIT rate: Table 16, MOS ASIC circuits, Full Custom
- Production year for die FIT rate: 2009
- Integration Density: 50-5k
- IEC62380 part and section for package FIT rate: Table 17b, Peripheral Connection Packages
- Package type: TDFN 6 pins, length: 3mm, width: 3mm, pitch: 0.95mm
- Interface device (EOS relevant): No

The FIT rates of MAX16059 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT Rates According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	8.39
90%	13.39
95%	16.32
99%	22.84

Note 3: The FIT rates for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 3,945
- Number of Failures: 1
- Activation Energy: 0.7eV
- Raw Device Hours: 3,773,784
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 290,592,810

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for MAX16059 as derived from the component die area ratio and complexity, and from engineering expertise.

Since some failures had no effect and do not contribute to any failure mode, the total percentage of the Failure Mode Distribution would not add up to 100%. A Correction factor (CF) was applied to the distribution to account for failures with no effect on the system.

System Function

- Assert $\overline{\text{RESET}}$ when supply undervoltage (UV) fault is detected.

Table 3-1 Failure Mode Distribution (CF = 1.40)

Failure Modes	Failure Mode Distribution
$\overline{\text{RESET}}$ always asserted	28%
$\overline{\text{RESET}}$ never asserts	49%
$\overline{\text{RESET}}$ asserts at a higher voltage threshold	12%
$\overline{\text{RESET}}$ asserts at a lower voltage threshold	10%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX16059. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX16059. Refer to the product datasheet for a detailed description of each pin's function.

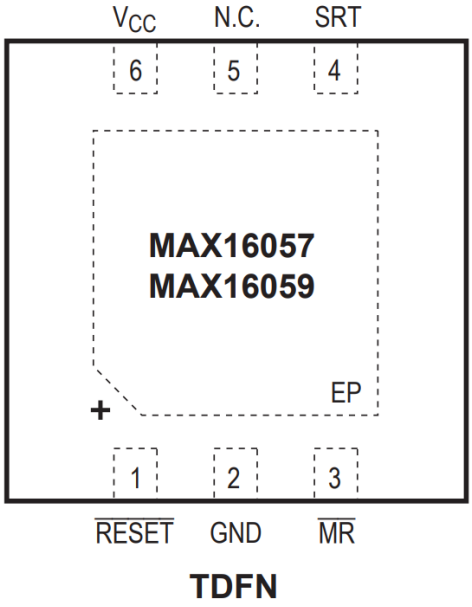

Figure 4-1. MAX16059 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA, based on the Typical Application Circuit, unless otherwise noted:

- The $\overline{\text{RESET}}$ pin is an active-low reset output available in open-drain configuration.
- The operating voltage range (VCC) is from 1.1V to 5.5V, and the operating temperature range (T_A) is from -40°C to +125°C.

Table 4-1 Pin FMEA for MAX16059 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ always high
2	GND	Part not functional
3	$\overline{\text{MR}}$	No $\overline{\text{RESET}}$ response when $\overline{\text{MR}}$ forced low
4	SRT	Incorrect reset timeout period. Part never asserts $\overline{\text{RESET}}$
5	N.C.	No effect
6	VCC	No effect

Table 4-2 Pin FMEA for MAX16059 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ always low
2	GND	No effect
3	$\overline{\text{MR}}$	$\overline{\text{RESET}}$ always low
4	SRT	Incorrect reset timeout period. Part always asserts $\overline{\text{RESET}}$
5	N.C.	No effect
6	VCC	Part not functional

Table 4-3 Pin FMEA for MAX16059 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	$\overline{\text{RESET}}$	Unreliable $\overline{\text{RESET}}$ output
2	GND	Part not functional
3	$\overline{\text{MR}}$	No $\overline{\text{RESET}}$ response when $\overline{\text{MR}}$ forced low
4	SRT	Incorrect reset timeout period. Part never asserts $\overline{\text{RESET}}$
5	N.C.	No effect
6	VCC	Part not functional

Table 4-4 Pin FMEA for MAX16059 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	$\overline{\text{RESET}}$	GND	$\overline{\text{RESET}}$ always low
2	GND	$\overline{\text{MR}}$	$\overline{\text{RESET}}$ always low
3	$\overline{\text{MR}}$	SRT	Incorrect reset timeout period. Part stays in $\overline{\text{RESET}}$ when $\overline{\text{MR}}$ is low. Part never asserts $\overline{\text{RESET}}$ when $\overline{\text{MR}}$ is high
4	SRT	N.C.	No effect
5	N.C.	VCC	No effect
6	VCC	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ always high

5 | Revision History

Revision	Revision Date	Description
A	October 2024	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

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