

RELIABILITY REPORT FOR MAXQ7666BATM+

PLASTIC ENCAPSULATED DEVICES

February 8, 2011

MAXIM INTEGRATED PRODUCTS

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| Approved by |
|----------------------|
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| Quality Assurance |
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Conclusion

The MAXQ7666BATM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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- I. Device Description
 - A. General

The MAXQ7666 smart systems-on-a-chip (SoC) is a data-acquisition system based on a microcontroller (iC). As a member of the MAXQ® family of 16-bit reduced instruction set computing (RISC) iCs, the MAXQ7666 is ideal for low-cost, low-power, embedded applications such as automotive, industrial controls, and building automation. The flexible, modular architecture design used in this iC allows targeted product development for specific applications with minimal effort. The MAXQ7666 incorporates a high-performance 16-bit RISC core, a 12-bit 500ksps SAR ADC with a programmable-gain amplifier (PGA), a 12-bit DAC with a buffered voltage output, and a full CAN 2.0B controller, supporting transfer rates up to 1Mbps. The device includes an internal crystal oscillator that drives an external crystal of 8MHz for the system clock. An internal 7.6MHz RC oscillator provides an alternate system clock. The MAXQ7666 includes an internal temperature sensor to measure die temperature and an external temperature-sensor driver. The analog functions and digital I/O operate from a +5V supply, while the internal digital core operates from a +3.3V supply. An internal linear regulator can provide +3.3V to the digital supply if an external +3.3V supply is not available. The MAXQ7666 also includes two power supply supervisors and a JTAG interface for in-system programming and debugging. The device includes 16KB (8K x 16) of program flash memory, up to 512 bytes (256 x 16) of data flash, and 512 bytes (256 x 16) of RAM. The MAXQ7666 is available in a 48-pin TQFN (7mm x 7mm) package and is specified to operate from -40°C to +125°C.



II. Manufacturing Information

| A. Description/Function: | 16-Bit, RISC, Microcontroller-Based, Smart Data-Acquisition System |
|----------------------------------|---|
| B. Process: | S45 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | California, Texas or Japan |
| E. Assembly Location: | Thailand |
| F. Date of Initial Production: | January 18, 2010 |
| III. Packaging Information | |
| A. Package Type: | 48-pin TQFN 7x7 |

| , i · conago ·)poi | |
|---|--------------------------|
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #31-4831 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | N/A |
| K. Single Layer Theta Jc: | N/A |
| L. Multi Layer Theta Ja: | 27°C/W |
| M. Multi Layer Theta Jc: | 1.5°C/W |
| | |

IV. Die Information

| A. Dimensions: | 209 X 203 mils |
|----------------------------|---|
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |
| | |



V. Quality Assurance Information

| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA) |
|-----------------------------------|---|
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{1000 \text{ x } 4340 \text{ x } 143 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}$ $\chi = 1.5 \text{ x } 10^{-9}$ $\lambda = 1.5 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NDVTCAA D/C 0817)

The UC31 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA.



Table 1 Reliability Evaluation Test Results

MAXQ7666AATM+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|--------------------|------------------|---------------------------|-------------|-----------------------|-------------------|
| Static Life Test (| Note 1) | | | | |
| | Ta = 135°C | DC Parameters | 48 | 0 | NDGBAC, D/C 0801 |
| | Biased | & functionality | 47 | 0 | NDGTBAD, D/C 0801 |
| | Time = 1000 hrs. | | 48 | 0 | NDGTBAB, D/C 0801 |

Note 1: Life Test Data may represent plastic DIP qualification lots.