RELIABILITY REPORT

FOR

MAX984ESE+T

PLASTIC ENCAPSULATED DEVICES

August 18, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX984ESE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX971-MAX974 and MAX981-MAX984 single/dual/quad low-voltage comparators feature the lowest power consumption available. These micropower devices draw less than 4µA supply current over temperature (MAX971/MAX972/MAX981/MAX982), and include an internal 1.182V ±1% (MAX971/MAX973/ MAX974) or ±2% (MAX981-MAX984) voltage reference and programmable hysteresis. Ideal for 3V or 5V single-supply applications, these devices operate from a single 2.5V to 11V supply (or ±1.25V to ±5.5V dual supplies), and each comparator's input voltage ranges from the negative supply rail to within 1.3V of the positive supply. The single MAX971/MAX981 and the dual MAX973/ MAX982/MAX983 provide a unique, simple method for adding hysteresis without feedback or complicated equations, simply by using the HYST pin plus two resistors. The MAX971-MAX974 and MAX981-MAX984's open-drain outputs permit wire-ORed configurations. Thanks to an 11V output range and separate GND pin for the output transistor (MAX971/MAX974, MAX981/MAX984), these devices are ideal for level translators and bipolar to single-ended converters. For similar devices with complementary output stages, see the MAX921-MAX924 (1% reference) and the MAX931-MAX934 (2% reference).

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II. Manufacturing Information

A. Description/Function:	Ultra-Low-Power, Open-Drain, Single/Dual-Supply Comparators
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines and Thailand
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1501-0107
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	115°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	75°C/W
M. Multi Layer Theta Jc:	24°C/W

IV. Die Information

A. Dimensions:	70 X 110 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.9 \times 10^{-9}$

λ = 6.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.03 @ 25C and 0.57 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NNYBCA420C, D/C 1304)

The CM31-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX984ESE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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