RELIABILITY REPORT

FOR

MAX9700xExx

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

July 21, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX9700 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9700 mono class D audio power amplifier provides class AB amplifier performance with class D efficiency, conserving board space and extending battery life. Using a class D architecture, the MAX9700 delivers 1.2W into an 8Ω load while offering efficiencies above 90%. A patented, low-EMI modulation scheme renders the traditional class D output filter unnecessary.

The MAX9700 offers two modulation schemes: a fixed-frequency (FFM) mode, and a spread-spectrum (SSM) mode that reduces EMI-radiated emissions due to the modulation frequency. Furthermore, the MAX9700 oscillator can be synchronized to an external clock through the SYNC input, allowing the switching frequency to be user defined. The SYNC input also allows multiple MAX9700s to be cascaded and frequency locked, mini-mizing interference due to clock intermodulation. The device utilizes a fully differential architecture, a full-bridged output, and comprehensive click-and-pop suppression. The gain of the MAX9700 is set internally (MAX9700A: 6dB, MAX9700B: 12dB, MAX9700C: 15.6dB, MAX9700D: 20dB), further reducing external component count.

The MAX9700 features high 72dB PSRR, a low 0.01% THD+N, and SNR in excess of 90dB. Short-circuit and thermal-overload protection prevent the device from damage during a fault condition. The MAX9700 is avail-able in 10-pin TDFN (3mm x 3mm x 0.8mm), 10-pin µMAX, and 12-bump UCSP™ (1.5mm x 2mm x 0.6mm) packages. The MAX9700 is specified over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	6V
PVDD to PGND	6V
GND to PGND	-0.3V to +0.3V
All Other Pins to GND	-0.3V to (VDD + 0.3V)
Continuous Current Into/Out of PVDD/PGND/OUT_	±600mA
Continuous Input Current (all other pins)	±20mA
Duration of OUT_ Short Circuit to GND or PVDD	Continuous
Duration of Short Circuit Between OUT+ and OUT-	Continuous
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Reflow	+235°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin DFN	1951mW
10-Pin µMAX	444mW
12-Bump UCSP	484mW
Derates above +70°C	
10-Pin Dfn	24.4mW/°C
10-Pin µMAX	5.6mW/°C
12-Bump UCSP	6.1mW/°C

II. Manufacturing Information

A. Description/Function:	1.2W, Low-EMI, Filterless, Class D Audio Amplifier
B. Process:	B6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	3595
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Malaysia, Thailand or USA
F. Date of Initial Production:	October, 2003

III. Packaging Information

	10-Lead DFN	**10-Lead µMAX**	**12-Bump UCSP**
A. Package Type:			
B. Lead Frame:	Copper	Copper	N/A
C. Lead Finish:	Solder Plate or 100% Matte Tin		N/A
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-9000-0466	# 05-9000-0465	# 05-9000-0705
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	70 x 60 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.6 microns (as drawn)
F. Minimum Metal Spacing:	.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.91 \times 10^{-9}$ $\lambda = 22.91$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6183) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**). Current monitor data for the B6 Process results in a FIT rate of 0.28 @ 25°C and 4.88 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AU11 die type has been found to have all pins able to withstand a transient pulse of +/-2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9700xExx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	DFN uMAX UCSP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	DFN uMAX UCSP	77 77 N/A	0 0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters & functionality	TSSOP TQFN UCSP	77 77 77	0 0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

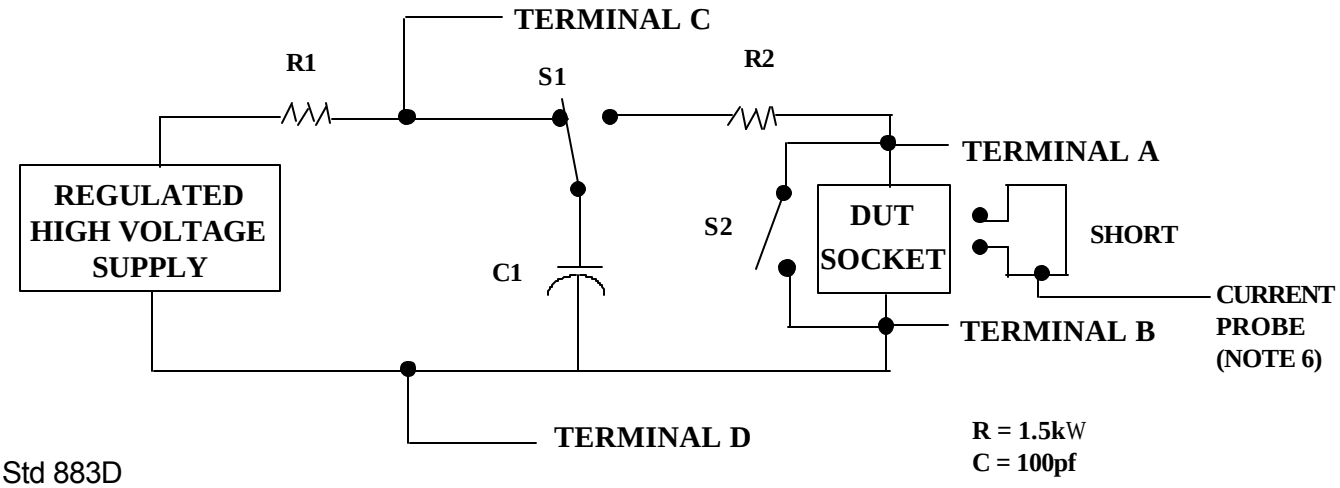
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

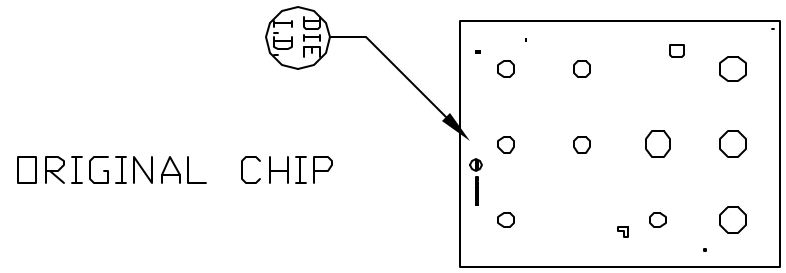
3.4 Pin combinations to be tested.

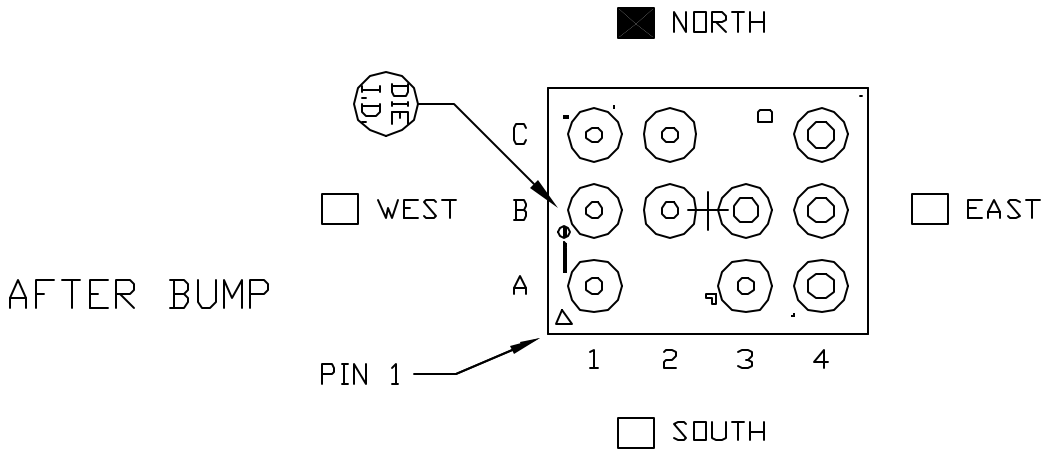
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

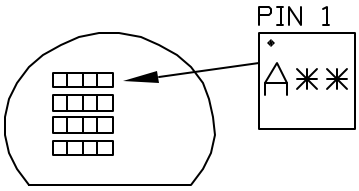
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







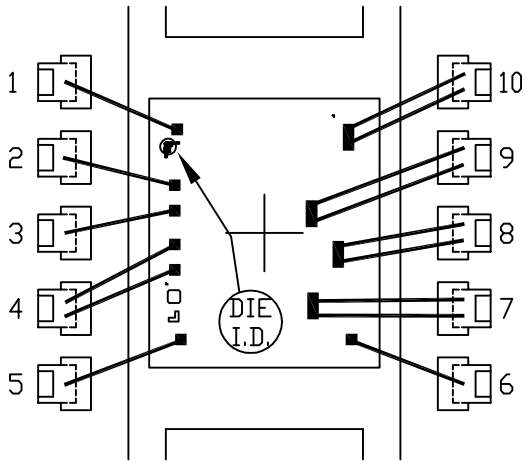
SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



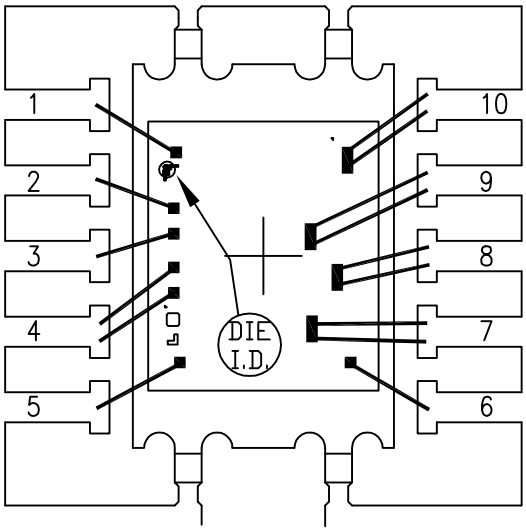
PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B12-11		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-9000-0705	REV: C
	DESIGN				

3x3x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



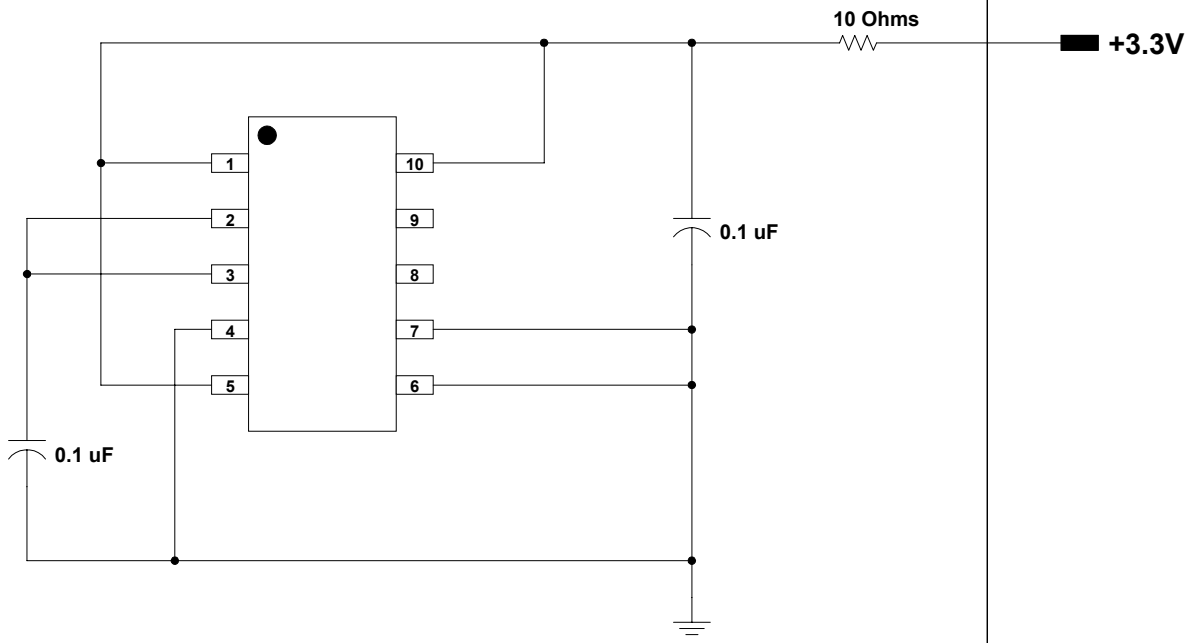
PKG. CODE: T1033-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71×102	PKG.			BOND DIAGRAM #: 05-9000-0466	REV: A
	DESIGN				



PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-9000-0465	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 9712/9700A/9700B/9700C/9700D/9705
PACKAGE: 10-uMAX
MAX. EXPECTED CURRENT = 5mA