RELIABILITY REPORT

FOR

MAX9598CTL+

PLASTIC ENCAPSULATED DEVICES

June 11, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX9598CTL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX9598 dual SCART matrix routes audio and video signals between a set-top box decoder chip and two external SCART connectors under I²C control. Operating from a 3.3V supply and a 12V supply, the MAX9598 consumes 70mW during quiescent operation and 471mW during average operation when driving typical signals into typical loads. Video input detection, video load detection, and a 1.7mW low-power mode facilitate the design of low-power set-top boxes. The MAX9598 audio section contains a buffered cross-point to route audio inputs to audio outputs. The DirectDrive® output amplifiers create a 2VRMS full-scale audio signal biased around ground, eliminating the need for bulky output capacitors and reducing click-and-pop noise. The zero-cross detection circuitry also further reduces clicks and pops by enabling audio sources to switch only during a zero-crossing. The MAX9598 video section contains a buffered cross-point to route video inputs to video outputs. The standard-definition video signals from the set-top box decoder chip are lowpass filtered to remove out-of-bandwidth artifacts. The MAX9598 also supports slow-switching and fast-switching signals. An interrupt signal from the MAX9598 informs the microcontroller (µC) when the system status has changed. The MAX9598 is available in a compact 40-pin thin QFN package and is specified over the 0°C to +70°C commercial temperature range.

II. Manufacturing Information

A. Description/Function:	Low-Power Audio/Video Switch for Dual SCART Connectors
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	ASAT China, UTL Thailand
F. Date of Initial Production:	January 25, 2008

III. Packaging Information

A. Package Type:	40-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	102 X 104 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Al/0.5% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.4 \times 10^{-9}$

λ = 13.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The VA68 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX9598CTL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data