RELIABILITY REPORT FOR

MAX9374EKA+T / MAX9374ESA+ / MAX9374AEKA+T / MAX9374AESA+

PLASTIC ENCAPSULATED DEVICES

January 18, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX9374EKA+T / MAX9374ESA+ / MAX9374AEKA+T / MAX9374AESA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9374 and MAX9374A are 2.0GHz differential LVPECL-to-LVDS translators and are designed for telecom applications. They feature 250ps propagation delay. The differential output conforms to the ANSI TIA/EIA-644 LVDS standard. The inputs are biased with internal resistors such that the output is differential low when inputs are open. An on-chip VBB reference output is available for single-ended operation. The MAX9374 is designed for low-voltage operation from a 2.375V to 2.625V power supply for use in 2.5V systems. The MAX9374A is designed for 3.0V to 3.6V operation in systems with a nominal 3.3V supply. Both devices are offered in industry-standard 8-pin SOT23 and SO packages.

II. Manufacturing Information

A. Description/Function:	Differential LVPECL-to-LVDS Translators	
B. Process:	GST2	
C. Number of Device Transistors:	16072	
D. Fabrication Location:	USA	
E. Assembly Location:	Malaysia, Thailand	Malaysia, Philippines, Thailand
F. Date of Initial Production:	January 26, 2002	

III. Packaging Information

A. Package Type:	8-pin SOT23	8-pin SOIC
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-3601-0027	#05-3601-0028
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Jb:	N/A°C/W	170°C/W
K. Single Layer Theta Jc:	N/A°C/W	40°C/W
L. Multi Layer Theta Ja:	195.8°C/W	136°C/W
M. Multi Layer Theta Jc:	70°C/W	38°C/W

IV. Die Information

A. Dimensions:	46 X 30 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 24.4 \times 10^{-9}$

$\lambda = 24.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.03 @ 25°C and 0.48 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot N9H1AQ001B, D/C 0146)

The EC21-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX9374EKA+T / MAX9374ESA+ / MAX9374AEKA+T / MAX9374AESA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0	N9H1AQ001C, D/C 0146

Note 1: Life Test Data may represent plastic DIP qualification lots.