RELIABILITY REPORT

FOR

MAX9286GTN+

PLASTIC ENCAPSULATED DEVICES

June 5, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX9286GTN+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9286 Gigabit multimedia serial link (GMSL) deserializer receives data from up to four GMSL serializers over 50Î© coax or 100Î© shielded twisted-pair (STP) cables and output data on four CSI-2 lanes. Each serial link has an embedded control channel operating from 9.6kbps to 1Mbps in UART-to-UART, UART-to-I²C, and I²C-to-I²C mode. Using the control channel, a Î¼C can program the serializers, deserializer, and peripheral device registers at any time, independent of video timing. A maskable broadcast write speeds programming of image sensor registers. For use with longer cables, the deserializer has a programmable cable equalizer and programmable error detection and correction. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.7V to 1.9V and the I/O supply is 1.7V to 3.6V. The device is available in lead(Pb)-free, 56-pin, 8mm x 8mm QFND and TQFN packages with exposed pad and 0.5mm lead pitch.

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II. Manufacturing Information

A. Description/Function:	Quad 1.5Gbps GMSL Deserializer with Coax or STP Input and CSI-2 Output
B. Process:	TS18
C. Number of Device Transistors:	4802277
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	May 22, 2015
1997	

III. Packaging Information

A. Package Type:	56L TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-100083
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	213.7795X213.7795 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{500 \times 4340 \times 239 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.77 \times 10^{-9}$

λ = 1.77 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot QAXJ6Q002A, D/C 1447)

The HS67-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of+/-100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX9286GTN+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 500 hrs.	DC Parameters & functionality	80 79 80	0 0 0	QAXJ6Q002A, D/C 1447 QAXJ6Q003A, D/C 1447 QAXJ6A004A, D/C 1447

Note 1: Life Test Data may represent plastic DIP qualification lots.

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