

RELIABILITY REPORT
FOR
MAX9163ESA+
PLASTIC ENCAPSULATED DEVICES

February 2, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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| Approved by |
| Ken Wendel |
| Quality Assurance |
| Director, Reliability Engineering |

Conclusion

The MAX9163ESA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9163 high-speed bus low-voltage differential signaling (BLVDS) transceiver is designed specifically for heavily loaded multipoint bus applications. The MAX9163 operates from a single 3.3V power supply, and is pin compatible with the DS92LV010A. The transceiver consists of one differential BLVDS line driver and one LVDS receiver. The driver output and receiver input are connected internally to minimize bus loading. The individual enable logic inputs (DE, active-low RE) are used to enable the driver or the receiver. The MAX9163 driver output uses a current-steering configuration to generate a 9mA (typ) drive current. The driver accepts a single-ended input and translates it to a differential output level of 243mV (typ) into 27 Ω at speeds up to 200Mbps. The MAX9163 receiver detects a differential input as low as 100mV and translates it to a single-ended output at speeds up to 200Mbps. The receiver input features a fail-safe circuit that sets the receiver output high when the receiver inputs are undriven and open, terminated, or shorted. The MAX9163 is offered in an 8-lead SO package, and is specified for operation from -40°C to +85°C.

II. Manufacturing Information

| | |
|----------------------------------|----------------------------------|
| A. Description/Function: | Bus LVDS 3.3V Single Transceiver |
| B. Process: | TS35 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Taiwan |
| E. Assembly Location: | Malaysia, Philippines, Thailand |
| F. Date of Initial Production: | January 25, 2003 |

III. Packaging Information

| | |
|--|--------------------------|
| A. Package Type: | 8-pin SOIC (N) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-0345 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 170°C/W |
| K. Single Layer Theta Jc: | 40°C/W |
| L. Multi Layer Theta Ja: | 128.4°C/W |
| M. Multi Layer Theta Jc: | 36°C/W |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 49 X 70 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.35µm |
| F. Minimum Metal Spacing: | 0.35µm |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS20 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX9163ESA+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|-------------------------------|-------------|--------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 48 | 0 |
| Moisture Testing (Note 2) | | | | |
| HAST | Ta = 130°C RH = 85% Biased Time = 96hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data