RELIABILITY REPORT

FOR

MAX9160EUI+

PLASTIC ENCAPSULATED DEVICES

June 30, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX9160EUI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX9160 125MHz, 14-port LVTTL/LVCMOS clock driver repeats the selected LVDS or LVTTL/LVCMOS input on two output banks. Each bank consists of seven LVTTL/LVCMOS series terminated outputs and a bank enable. The LVDS input has a fail-safe function. The MAX9160 has a propagation delay that can be adjusted using an external resistor to set the bias current for an internal delay cell. The LVTTL/LVCMOS outputs feature 200ps maximum output-to-output skew and ±100ps maximum added peak-to-peak jitter. The MAX9160 is designed to operate with a 3.3V supply voltage over the extended temperature range of -40°C to +85°C. This device is available in 28-pin exposed- and nonexposed-pad TSSOP and 32-lead 5mm x 5mm QFN packages.

II. Manufacturing Information

A. Description/Function:	LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	April 27, 2002

III. Packaging Information

A. Package Type:	28-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2801-0036
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	78°C/W
K. Single Layer Theta Jc:	12.5°C/W
L. Multi Layer Theta Ja:	71.6°C/W
M. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	72 X 70 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 24.4 \times 10^{-9}$

λ = 24.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS18 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX9160EUI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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