RELIABILITY REPORT

FOR

MAX9129ExE

PLASTIC ENCAPSULATED DEVICES

April 26, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX9129 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9129 is a quad bus low-voltage differential signaling (BLVDS) driver with flow-through pinout. This device is designed to drive a heavily loaded multipoint bus with controlled transition times (1ns 0% to 100% minimum) for reduced reflections. The MAX9129 accepts four LVTTL/LVCMOS input levels and translates them to output levels of 250mV to 450mV (standard LVDS levels) into a 27Ω load at speeds up to 200Mbps (100MHz).

The power-on reset ensures that all four outputs are disabled and high impedance during power up and power down. The outputs can be set to high impedance by two enable inputs, EN and EN-bar, thus dropping the device to a low-power state of 11mW. The enables are common to all four drivers. The flow-through pinout simplifies PC board layout and reduces crosstalk by keeping the LVTTL/LVCMOS inputs and BLVDS outputs separated.

The MAX9129 operates from a single +3.3V supply and is specified for operation from -40°C to +85°C. It is available in 16-pin QFN and TSSOP packages. Refer to the MAX9121 data sheet for a quad LVDS line receiver with flow-through pinout.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +4.0V
IN_, EN, EN to GND	-0.3V to (VCC + 0.3V)
OUT_+, OUT_- to GND	-0.3V to +4.0V
Short-Circuit Duration (OUT_+, OUT_-)	Continuous
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
ESD Protection	
Human Body Model, OUT_+, OUT_-	±8kV
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QFN	1481mW
16-Pin TSSOP	755mW
Derates above +70°C	
16-Pin QFN	18.5mW/°C
16-Pin TSSOP	9.4mW/°C

II. Manufacturing Information

A. Description/Function:	Quad Bus LVDS Driver withFlow-Through Pinout
B. Process:	TC35
C. Number of Device Transistors:	948
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand, Korea or Philippines
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	**16-Pin QFN**	**16-Pin TSSOP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-2801-0025	#05-2801-0026
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1	Level 1

IV. Die Information

A. Dimensions:	60 x 60 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5842) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The HS14 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9129ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN TSSOP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

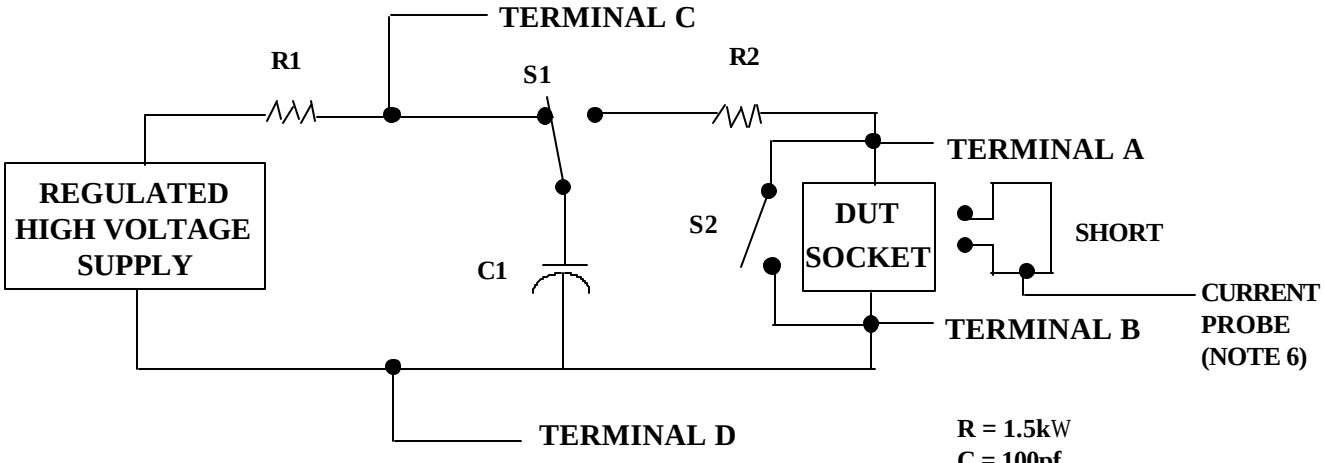
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

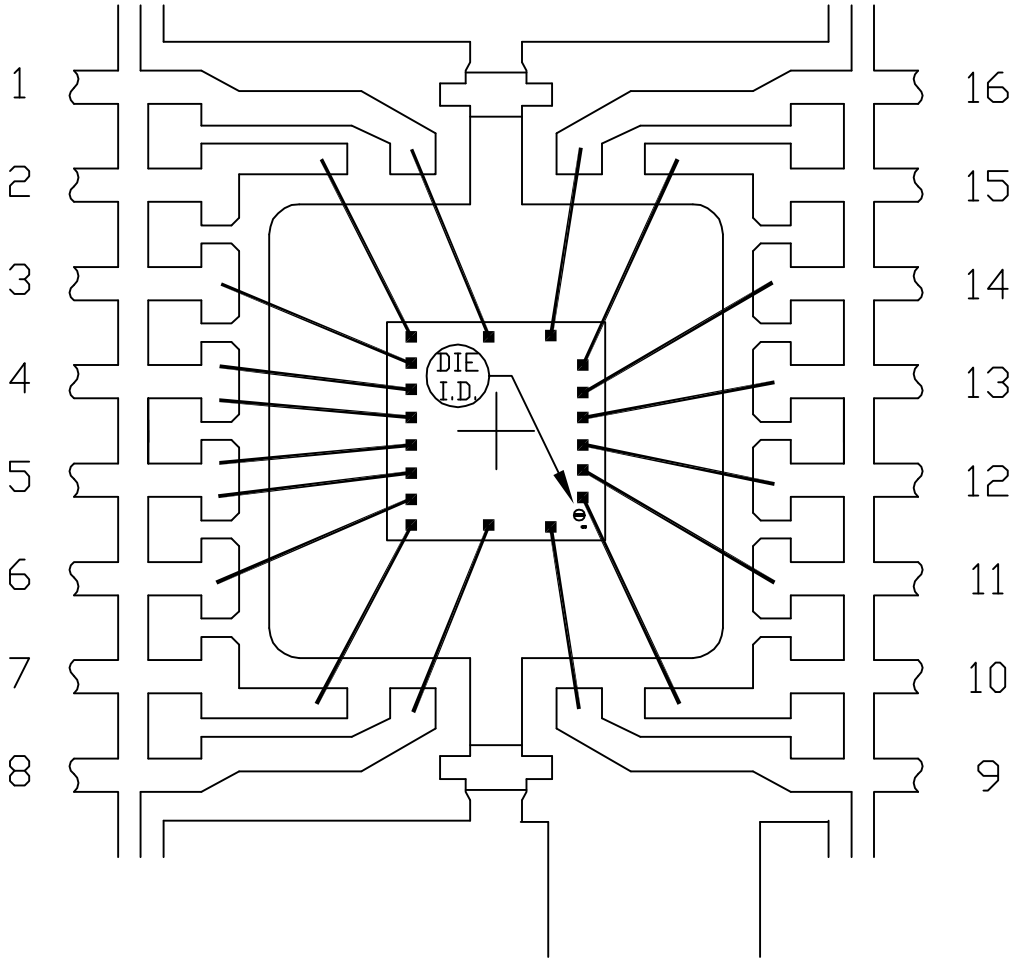
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

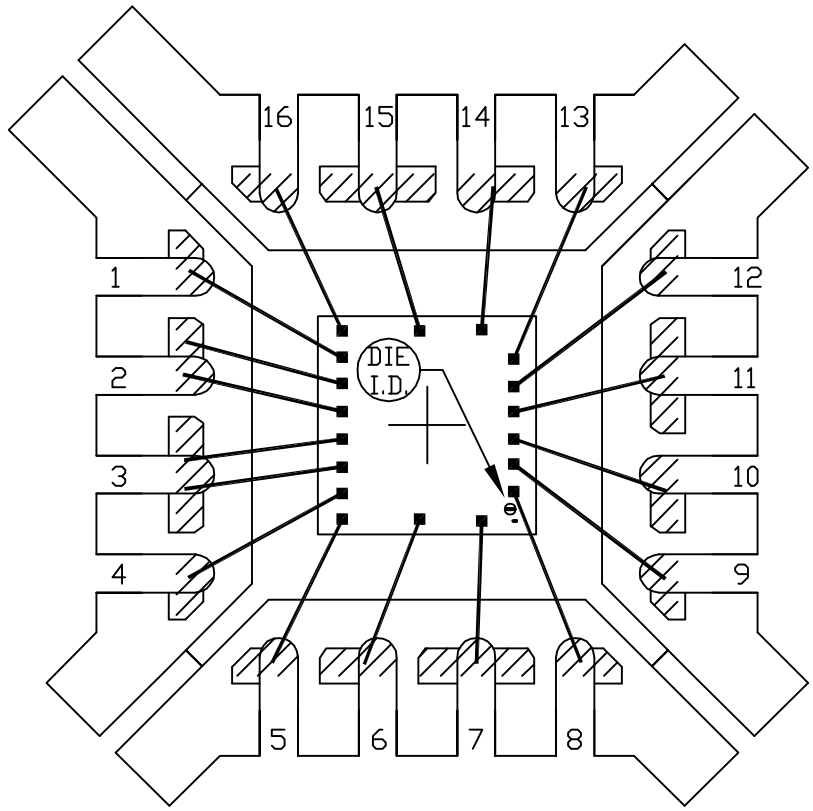


Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: U16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118X118	PKG.			BOND DIAGRAM #: 05-2801-0026	REV: A
	DESIGN				

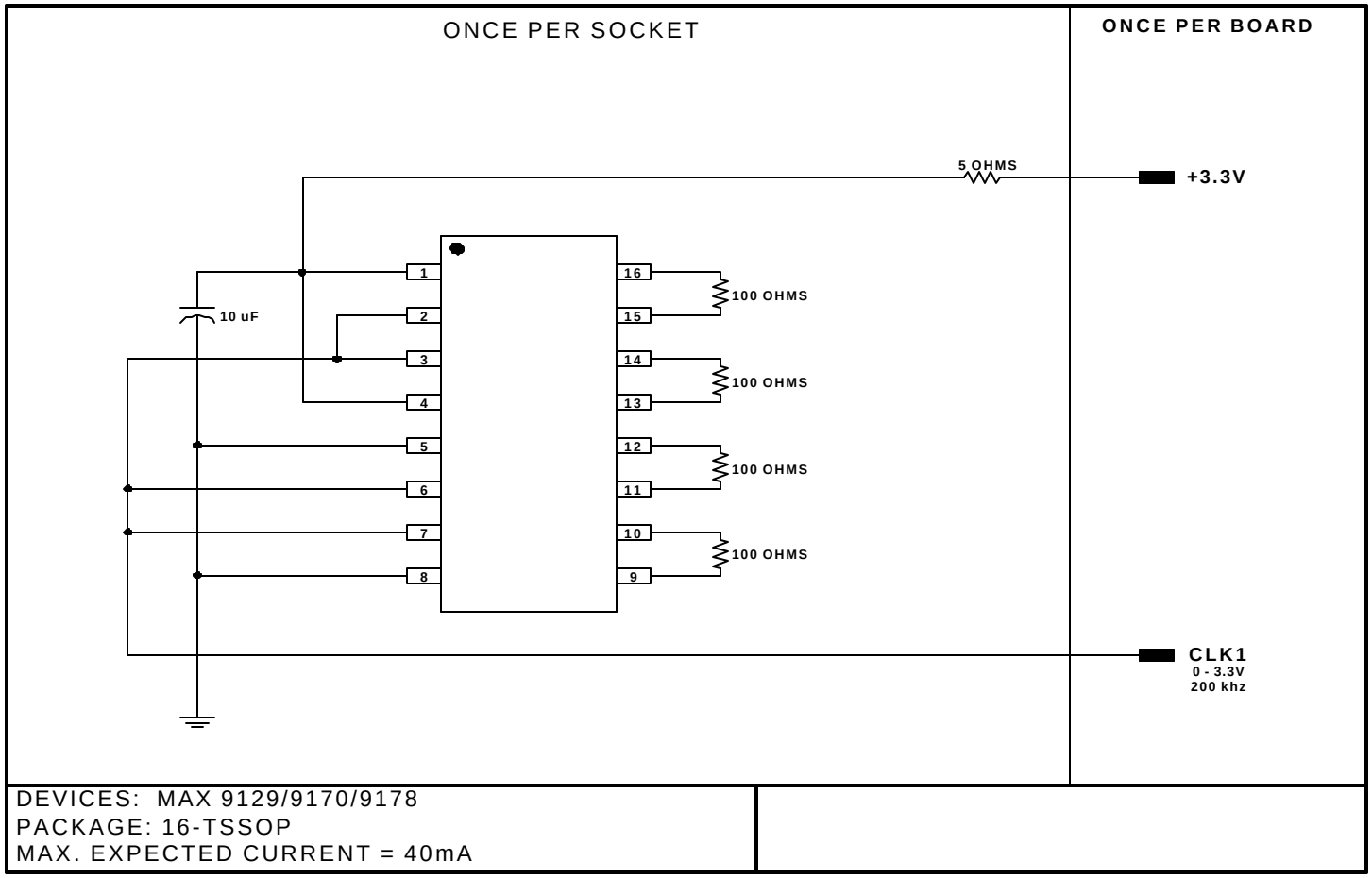
EXPOSED PAD PKG.



BONDABLE AREA

PKG. BODY SIZE: 4x4 mm

PKG. CODE: G1644-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 91x91	PKG.			BOND DIAGRAM #: 05-2801-0025	REV: A
	DESIGN				



DEVICES: MAX 9129/9170/9178
PACKAGE: 16-TSSOP
MAX. EXPECTED CURRENT = 40mA