MAX8548EUB
Rev. A

RELIABILITY REPORT

FOR

MAX8548EUB

PLASTIC ENCAPSULATED DEVICES

August 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX8548 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8548 is a voltage-mode pulse-width-modulated (PWM), step-down DC-DC controller ideal for a variety of cost-sensitive applications. It drives low-cost N-channel MOSFETs for both the high-side switch and synchronous rectifier, and require no external current-sense resistor. This device can supply output voltages as low as 0.8V.

The MAX8548 has a wide 2.7V to 28V input range, and does not need any additional bias voltage. The output voltage can be precisely regulated from 0.8V to 0.83 x V_{IN}. This devices can provide efficiency up to 95%. Lossless short-circuit and current-limit protection is provided by monitoring the RDS(ON) of the low-side MOSFET. The MAX8548 has a current-limit threshold of 165mV. The device features foldback-current capability to minimize power dissipation under short-circuit condition. Pulling the COMP/EN pin low with an open-collector or low-capacitance, open-drain device can shut down the device.

The MAX8548 has a current-limit threshold of 320mV. The device features foldback-current capability to minimize power dissipation under short-circuit condition. Pulling the COMP/EN pin low with an open-collector or low-capacitance, open-drain device can shut down all devices.

The MAX8548 operates at 100kHz. The MAX8548 is compatible with low-cost aluminum electrolytic capacitors. Input undervoltage lockout prevents proper operation under power-sag operations to prevent external MOSFETs from overheating. Internal soft-start is included to reduce inrush current. This device is offered in space-saving 10-pin µMAX packages.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to GND unless otherwise noted.)	
VIN to GND	-0.3V to +30V
VCC to GND	-0.3V, lower of 6V or (VL + 0.3V)
FB to GND	-0.3V to +6V
BST to GND	-0.3V to +36V
VL, DL, COMP to GND	-0.3V to (VCC + 0.3V)
BST to LX	-0.3V to +6V
DH to LX	-0.3V to (VBST + 0.3V)
VL Short to GND	5s
LX to GND	0 to 30V
Input Current (any pin)	±50mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin µMAX	444mW
Derates above +70°C	
10-Pin µMAX	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	3007
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand, Philippines or Malaysia
F. Date of Initial Production:	July, 2003

III. Packaging Information

A. Package Type:	**10-Pin µMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-3501-0016
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	58 x 72 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Opertions)
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 125 \times 2}$$ (Chi square value for MTTF upper limit)

4389 ← Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 8.69 \times 10^{-9}$

λ = 8.69 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5856) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PM32-5 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8548EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		125	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

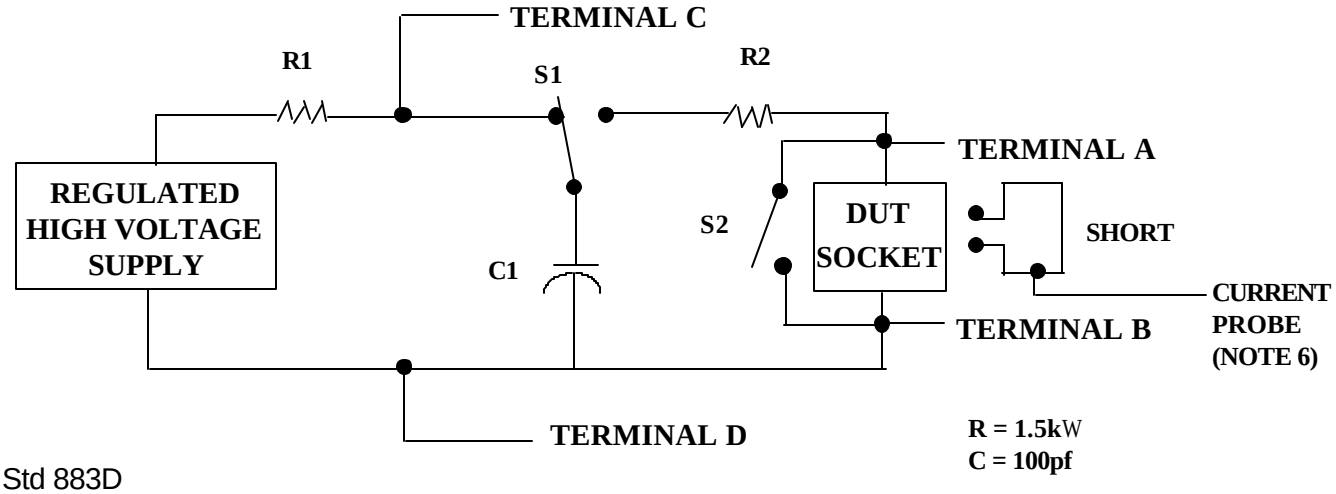
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

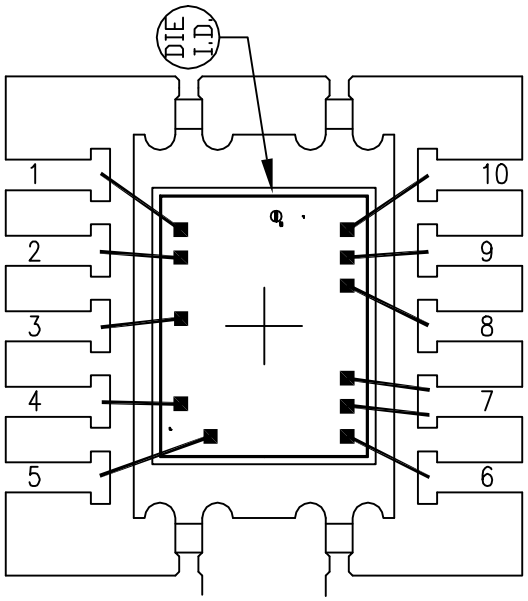
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



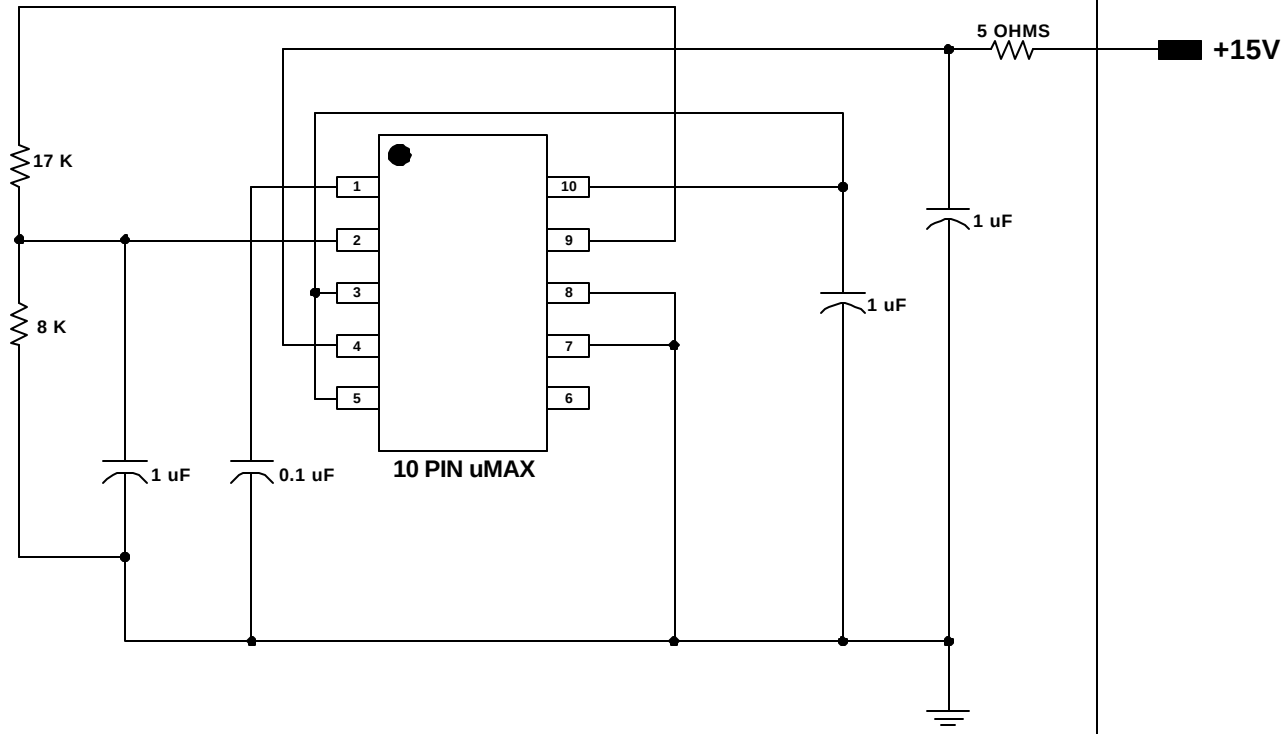
Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-3501-0016 / REV: A
	DESIGN			

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX1967EUB

MAX. EXPECTED CURRENT = 20mA

DRAWN BY: TEK TAN

NOTES: