RELIABILITY REPORT

FOR

MAX7365EWA70+T

WAFER LEVEL PRODUCTS

November 15, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX7365EWA70+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX7365 is an I²C-interfaced peripheral that provides microprocessors with management of up to 56 key switches. Key codes generated for each keypress and release enable easier implementation of multiple key entries. Key inputs monitored statically, not dynamically, ensure low-EMI operation. The switches can be metallic or resistive (carbon) with up to 5k of resistance. The device features autosleep and autowake to further minimize the power consumption of the device. The autosleep feature puts the device in a low-power state (1µA typ) after a programmable sleep timeout period. The autowake feature configures the device to return to normal operating mode from sleep upon a keypress. The key controller debounces and maintains a FIFO of keypress and release events (including autorepeat, if enabled). An interrupt (active-low INT) output can be configured to alert keypresses either as they occur or at the maximum rate. Unused key switches can be used as GPI. In addition, there are five additional general-purpose input/output (GPIO) ports. GPOs can be programmed as push-pull or open-drain to high- or low-side output drivers. When programmed as open drain, an optional on-chip 100k pullup/pulldown resister can be enabled. The device is available in a small (2mm x 2mm) 25-bump wafer-level package (WLP) for cell phones, pocket PCs, and other portable consumer electronic applications. The device operates over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	1MHz I²C-Interfaced 8 x 7 Key-Switch Controller with GPIO Ports
B. Process:	S18
C. Number of Device Transistors:	69558
D. Fabrication Location:	USA
E. Assembly Location:	Japan and USA
F. Date of Initial Production:	September 19, 2011

III. Packaging Information

A. Package Type:	25-bump WLP 5x5
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-4563
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	52°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	81.10 X 81.10 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot S2PZAQ001B, D/C 1121)

The DX51 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX7365EWA70+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	S2PZAQ001B, D/C 1121

Note 1: Life Test Data may represent plastic DIP qualification lots.