

RELIABILITY REPORT
FOR
MAX709SCUA+
PLASTIC ENCAPSULATED DEVICES

April 29, 2015

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX709SCUA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX709 provides a system reset during power-up, power-down, and brownout conditions. When VCC falls below the reset threshold, RESET goes low and holds the μP in reset for 140ms min after VCC rises above the threshold. The RESET output is guaranteed to be in the correct state with VCC down to 1V. The MAX709 provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, or +3V powered systems. The MAX709 is available 8-pin DIP, $\mu\text{MAX}^{\text{®}}$, and SO packages.

II. Manufacturing Information

A. Description/Function:	Power-Supply Monitor with Reset
B. Process:	B3
C. Number of Device Transistors:	300
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1701-0349
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	31X44 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 155 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 1.36 \times 10^{-9}$$

$\lambda = 1.36$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B3 Process results in a FIT Rate of 0.24 @ 25C and 4.22 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot IRHBCQ001M, D/C 0046)

The PW54-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX709SCUA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	75	0	NRHBB2199C, D/C 0418
	Biased	& functionality	80	0	NRHABA980K, D/C 0240
	Time = 1000 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.