

RELIABILITY REPORT  
FOR  
**MAX706RxxA**  
PLASTIC ENCAPSULATED DEVICES

July 17, 2006

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord". The signature is written in a cursive style with a large initial "J" and a long, sweeping underline.

Jim Pedicord  
Quality Assurance  
Manager, Reliability Operations

## Conclusion

The MAX706R successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

## I. Device Description

### A. General

The MAX706R microprocessor ( $\mu$ P) supervisory circuit reduces the complexity and number of components required to monitor +3V power-supply levels in +3V to +5V  $\mu$ P systems. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The MAX706R supervisory circuit provides the following four functions:

- 1) A reset output during power-up, power-down, and brownout conditions.
- 2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6s.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than the main supply.
- 4) An active-low, manual-reset input.

The MAX706R reset-threshold voltage level is 2.63V. It has active-low reset output signals.

The MAX708R/S/T provide the same functions as the MAX706R/S/T and MAX706AR/AS/AT except they do not have a watchdog timer. Instead, they provide both RESET-bar and RESET outputs. As with the MAX706, devices with R, S, and T suffixes have reset thresholds of 2.63V, 2.93V, and 3.08V, respectively.

This device is available in 8-pin SO, DIP, and  $\mu$ MAX® packages and is fully specified over the operating temperature range.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Terminal Voltage (with respect to GND)	
VCC	-0.3V to +6V
All Other Inputs (Note 1)	-0.3V to (VCC + 0.3V)
Input Current	
VCC	20mA
GND	20mA
Output Current (all outputs)	20mA
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP (derate 9.1mW/°C above +70°C)	727.3mW
8-Pin SO (derate 5.9mW/°C above +70°C)	470.6mW
8-Pin $\mu$ MAX (derate 4.5mW/°C above +70°C)	362mW
Operating Temperature Range	
MAX70_C	0°C to +70°C
MAX70_E	-40°C to +85°C
MAX70_M	-55°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

## II. Manufacturing Information

A. Description/Function:	+3V Voltage Monitoring, Low-Cost $\mu$ P Supervisory Circuits
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	572
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines, or Thailand
F. Date of Initial Production:	July, 1992

## III. Packaging Information

A. Package Type:	<b>8-pin <math>\mu</math>MAX</b>	<b>8-pin SO</b>	<b>8-pin PDIP</b>
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin (all packages)		
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0164	# 05-1701-0101	# 05-1701-100
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

## IV. Die Information

A. Dimensions:	70 x 65 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	$\text{SiO}_2$
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.87 \times 10^{-9} \quad \lambda = 6.87 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5934) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.15 @ 25C and 2.60 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PW27-4 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1000\text{V}$  per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX706RxxA**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test (Note 1)</b>					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	µMAX	77	0
			PDIP	77	0
			SO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

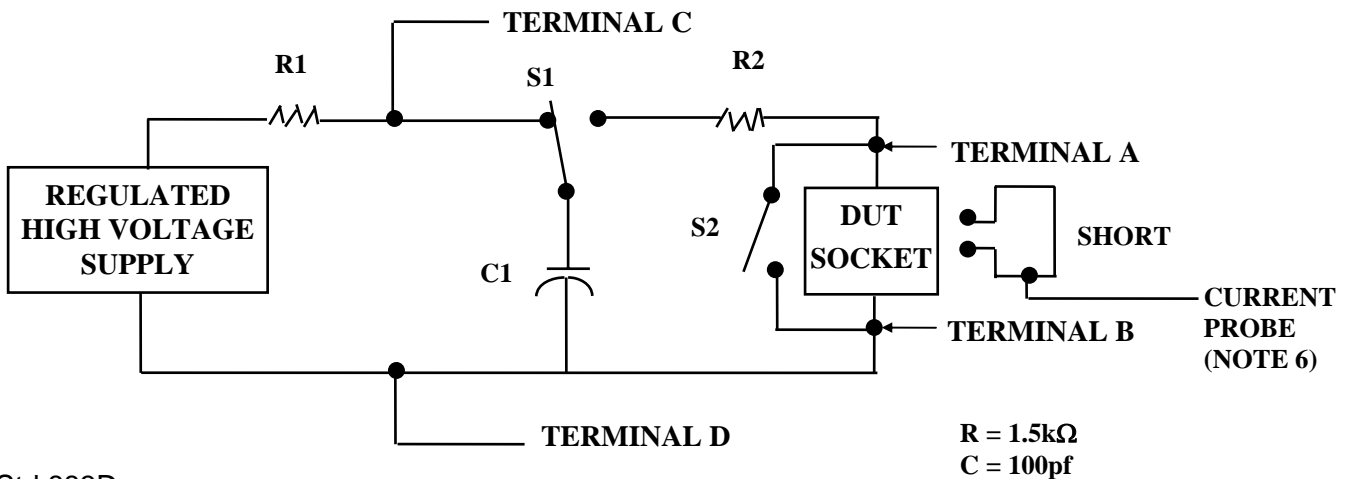
2/ No connects are not to be tested.

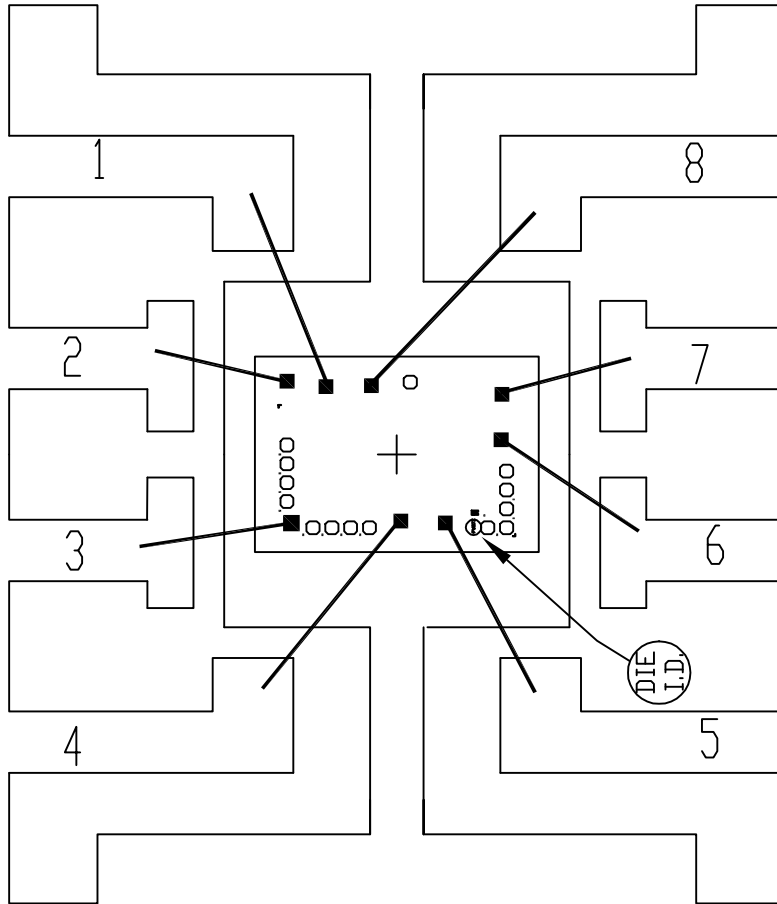
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

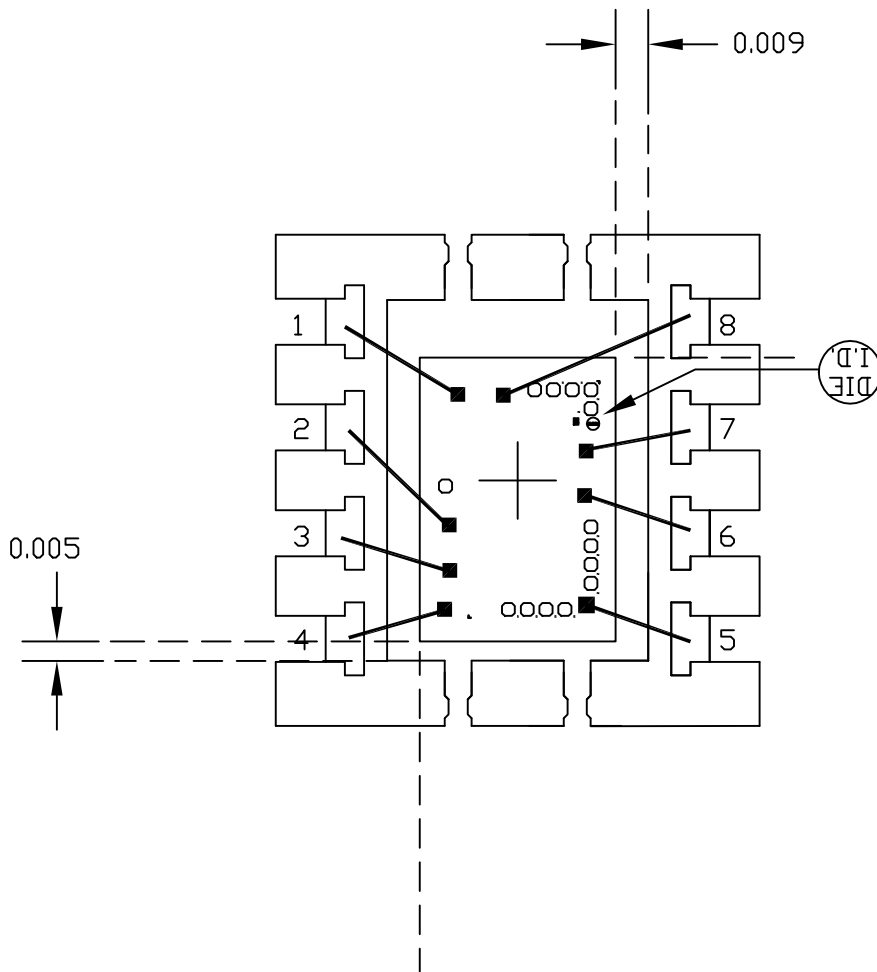
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



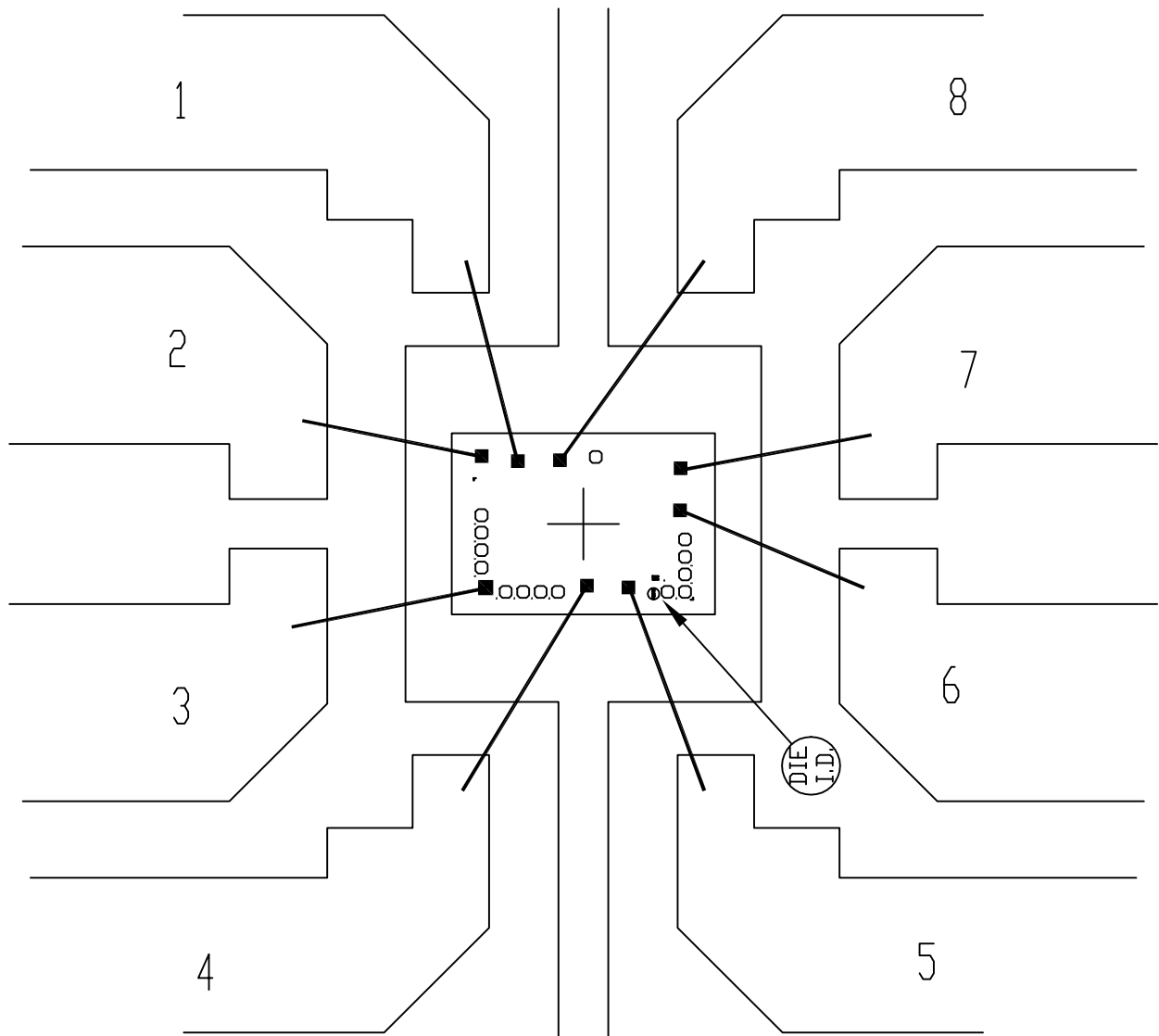


PKG. CODE: S8-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BOND DIAGRAM #: 05-1701-0101	REV: B



PKG. CODE: U8-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG. DESIGN			BOND DIAGRAM #: 05-1701-0164	REV: C





PKG. CODE: P8-1

SIGNATURES

DATE

**MAXIM**  
CONFIDENTIAL & PROPRIETARY

CAV./PAD SIZE:  
100 X 100

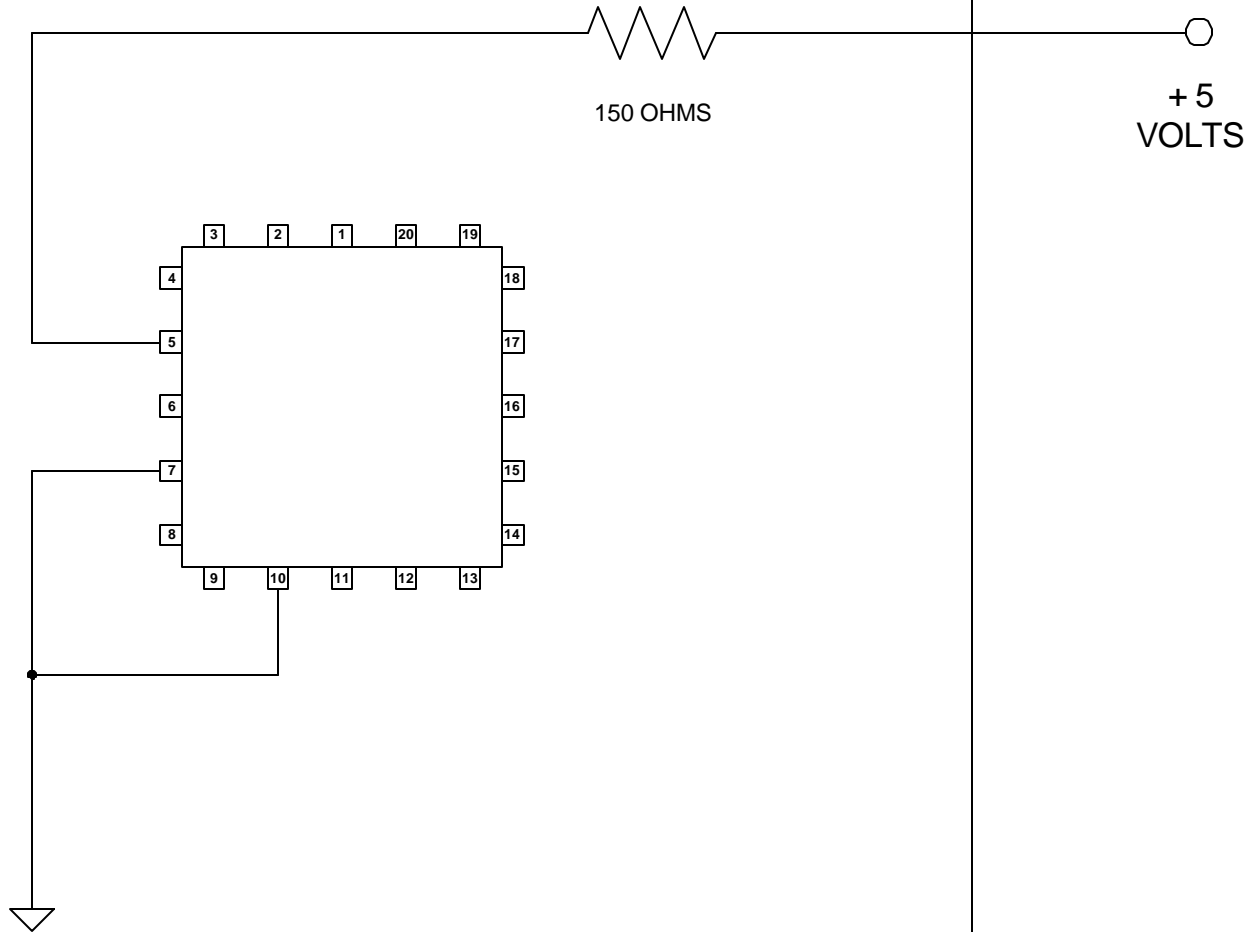
PKG.  
DESIGN

BOND DIAGRAM #:  
05-1701-0100

REV:  
B

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 705/706/707/708/813L  
PACKAGE: 20-LCC  
MAX. EXPECTED CURRENT = 300  $\mu$ A

NOTES: PW27Z-1Z