

FOR

MAX6718UKZGD3+

(MAX6715-MAX6729)

PLASTIC ENCAPSULATED DEVICES

April 9, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering



Conclusion

The MAX6718UKZGD3+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

IDevice Description	VQuality Assurance Information		
IIManufacturing Information	VIReliability Evaluation		
IIIPackaging Information	IVDie Information		
Attachments			

I. Device Description

A. General

The MAX6715-MAX6729 are ultra-low-voltage microprocessor (µP) supervisory circuits designed to monitor two or three system power-supply voltages. These devices assert a system reset if any monitored supply falls below its factory-trimmed or adjustable threshold and maintain reset for a minimum timeout period after all supplies rise above their thresholds. The integrated dual/triple supervisory circuits significantly improve system reliability and reduce size compared to separate ICs or discrete components. These devices monitor primary supply voltages (VCC1) from 1.8V to 5.0V and secondary supply voltages (VCC2) from 0.9V to 3.3V with factory-trimmed reset threshold voltage options (see Reset Voltage Threshold Suffix Guide). An externally adjustable RSTIN input option allows customers to monitor a third supply voltage down to 0.62V. These devices are guaranteed to be in the correct reset output logic state when either VCC1 or VCC2 remains greater than 0.8V. A variety of push-pull or open-drain reset outputs along with watchdog input, manual reset input, and power-fail input/output features are available (see Selector Guide). Select reset timeout periods from 1.1ms to 1120ms (min) (see Reset Timeout Period Suffix Guide). The MAX6715-MAX6729 are available in small 5, 6, and 8-pin SOT23 packages and operate over the -40°C to +85°C temperature range.



II. Manufacturing Information

Dual/Triple Ultra-Low-Voltage SOT23 µP Supervisory Circuits A. Description/Function:

B. Process: В8

C. Number of Device Transistors:

D. Fabrication Location: Texas

E. Assembly Location: Carsem Malaysia, ISPL Philippines, UTL Thailand, Unisem Malaysia

F. Date of Initial Production: January 26, 2002

III. Packaging Information

A. Package Type: 5-pin SOT23 B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin D. Die Attach: Conductive Epoxy E. Bondwire: Gold (1 mil dia.) Epoxy with silica filler F. Mold Material: G. Assembly Diagram: #05-9000-2051 H. Flammability Rating: Class UL94-V0 Level 1

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

324.3°C/W J. Single Layer Theta Ja: 82°C/W K. Single Layer Theta Jc:

IV. Die Information

A. Dimensions: 32 X 57 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide

Aluminum/Si (Si = 1%) C. Interconnect:

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn) F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq. H. Isolation Dielectric: SiO₂ I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 124 \times 2}$$
 (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$x = 8.7 \times 10^{-9}$$

% = 8.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B8 Process results in a FIT Rate of 2.71 @ 25C and 17.30 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The MS68-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.



Table 1

Reliability Evaluation Test Results

MAX6718UKZGD3+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test	(Note 1)				
	Ta = 135°C	DC Parameters	124	0	
	Biased	& functionality			
	Time = 192 hrs.				
Moisture Testing	(Note 2)				
85/85	Ta = 85°C	DC Parameters	77	0	
	RH = 85%	& functionality			
	Biased				
	Time = 1000hrs.				
Mechanical Stres	ss (Note 2)				
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles	& functionality			
•	Method 1010	•			

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data