RELIABILITY REPORT

FOR

MAX6664AEE

PLASTIC ENCAPSULATED DEVICES

June 17, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6664 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

MAX6664 is an ACPI-compliant local and remote-junction temperature sensor and fan controller. The device measures its own die temperature, as well as the temperature of a remote-PN junction and control the speed of a DC cooling fan based on the measured temperature. Remote temperature measurement accuracy is ±1°C from +60°C to +100°C. Temperature measurement resolution is 0.125°C for both local and remote temperatures.

Internal watchdog set points are provided for both local and remote temperatures. There are two comparison set points for local temperatures and two for remote temperatures. When a set point is crossed, the MAX6664 asserts either the INT-bar or THERM-bar outputs. These outputs can be used as interrupts, clock throttle signals, or overtemperature shutdown signals. The THERM-bar outputs for the MAX6664 can also function as inputs if either is pulled low to force the fan to full speed, unless this function is masked by the user.
The MAX6664 is available in 16-pin QSOP packages and operates over the -40°C to +125°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
All Voltages Are Referenced to GND	
TACH/AIN	-0.3V to +5.5V
VCC	-0.3V to +6V
DXP, ADD, CRIT0, CRIT1	-0.3V to + (VCC + 0.3V)
DXN	-0.3V to +0.8V
SMBDATA, SMBCLK, INT, THERM, FAN_FAULT, SDL, SDR	-0.3V to +6V
SMBDATA, INT, THERM, FAN_FAULT, PWM_OUT Current	-1mA to +50mA
DXN Current	±1mA
ESD Protection (all pins, Human Body Model)	2000V
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3 mW/°C

II. Manufacturing Information

A. Description/Function:	Temperature Monitors and PWM Fan Controller
B. Process:	S8
C. Number of Device Transistors:	27,074
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines and Thailand
F. Date of Initial Production:	April, 2003

III. Packaging Information

A. Package Type:	**16-QSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0134
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	86 x 136
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

192 x 4389 x 48 x 2 — Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6063) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The TS38-2 die type has been found to have all pins able to withstand a transient pulse of 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6664AEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

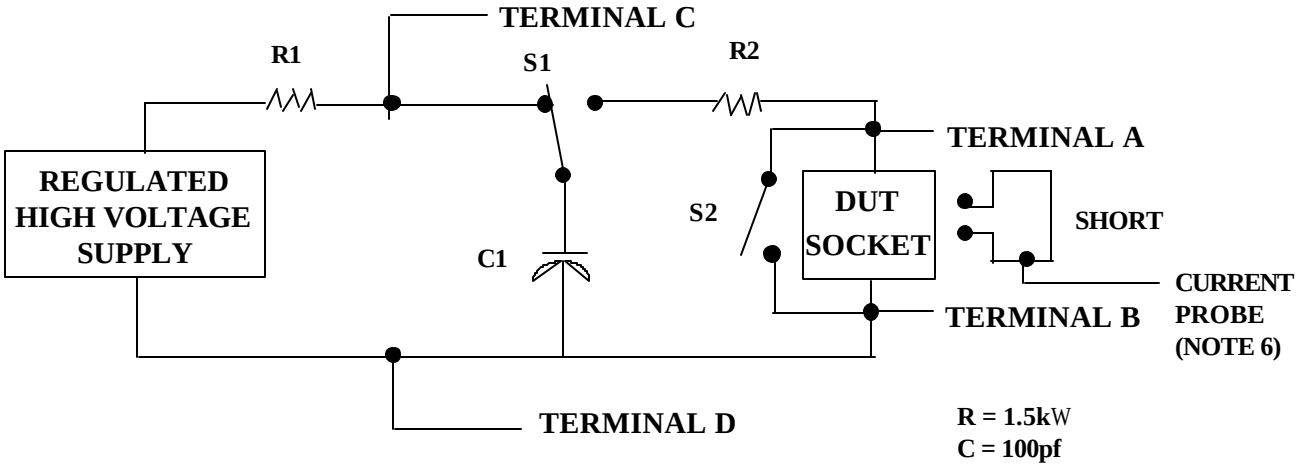
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

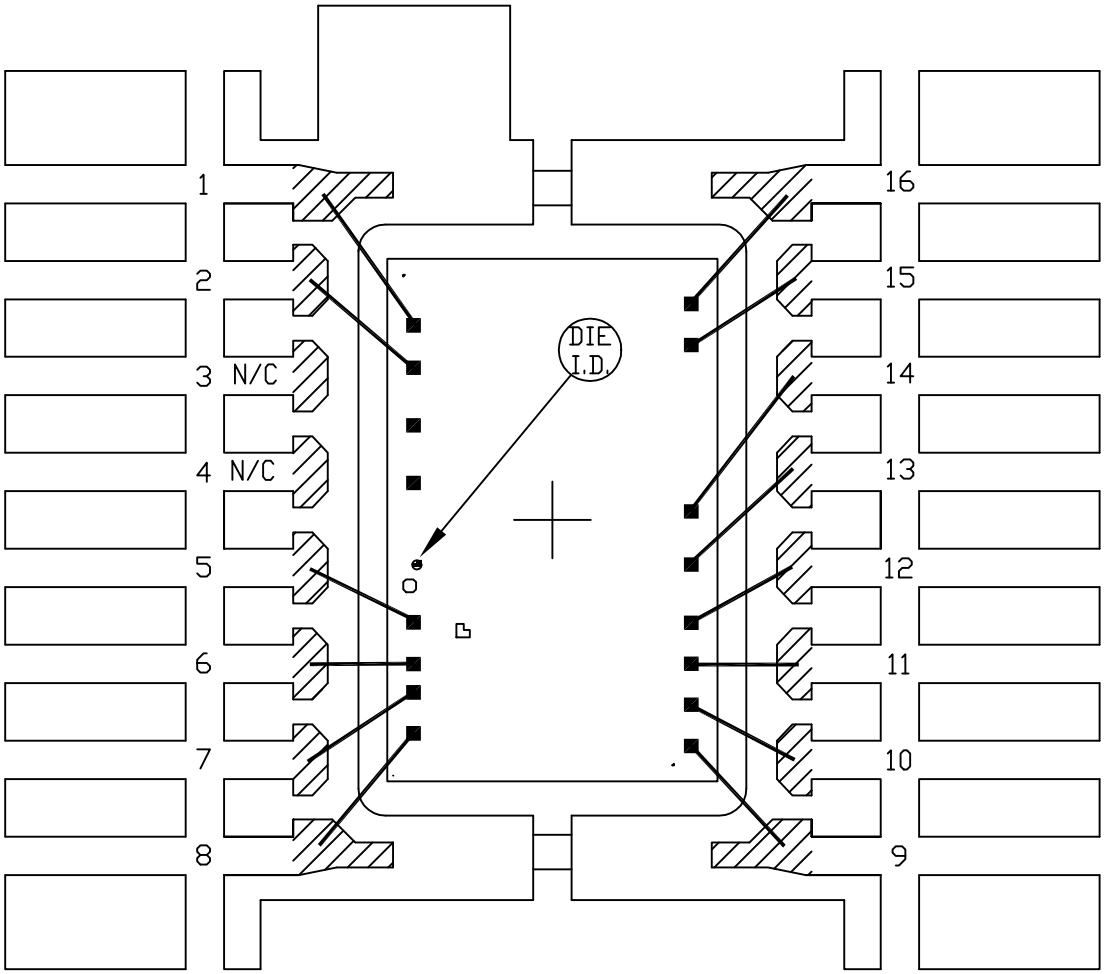
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

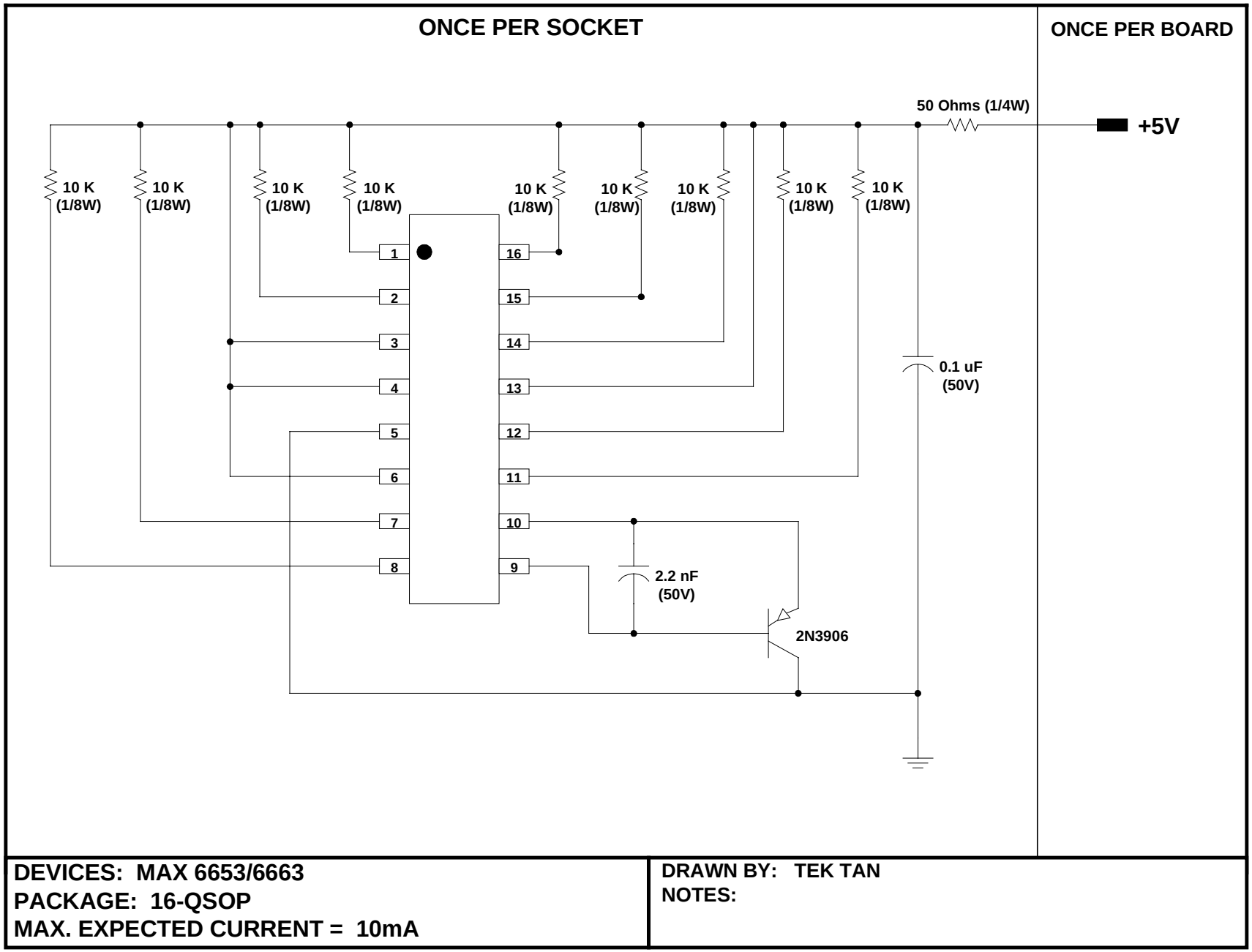
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





BONDABLE AREA

PKG. CODE: E16-5		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 101×154	PKG.			BOND DIAGRAM #: 05-9000-0134	REV: B
	DESIGN				



DEVICES: MAX 6653/6663
PACKAGE: 16-QSOP
MAX. EXPECTED CURRENT = 10mA

DRAWN BY: TEK TAN
NOTES: