MAX6504UKxxxx Rev. A

RELIABILITY REPORT

FOR

MAX6504UKxxxx

PLASTIC ENCAPSULATED DEVICES

July 12, 2006

MAXIM INTEGRATED PRODUCTS

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Written by

/en

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Conclusion

The MAX6504 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6504[†] low-cost, fully integrated temperature switch asserts a logic signal when its die temperature crosses a factory-programmed threshold. Operating from a +2.7V to +5.5V supply, this device features two on-chip, temperature-dependent voltage references and a comparator. They are available with factory-trimmed temperature trip thresholds from -45°C to +125°C in 10°C increments, and are accurate to ±0.5°C (typ) or ±6°C (max). This device requires no external components and typically consumes 30µA supply current. Hysteresis is pin-selectable at +2°C or +10°C.

The MAX6504 has an active high, push-pull output intended to directly drive fancontrol logic. The MAX6504 is offered with cold-temperature thresholds (-45°C to +15°C), asserting when the temperature is below the threshold.

The MAX6504 is offered in eight standard temperature versions; contact the factory for pricing and availability of nonstandard temperature versions. It is available in 5-pin SOT23 and 7-pin TO-220 packages.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VCC)	-0.3V to +7V
TOVER (MAX6501)	-0.3V to +7V
TOVER (MAX6502)	-0.3V to (VCC + 0.3V)
TUNDER (MAX6503)	-0.3V to +7V
TUNDER (MAX6504)	-0.3V to (VCC + 0.3V)
All Other Pins	-0.3V to (VCC + 0.3V)
Input Current (all pins)	20mA
Output Current (all pins)	20mA
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C)	571mW
Operating Temperature Range	-55°C to +135°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, +2.7V to +5.5V, Micropower Temperature Switches in SOT23 and TO-220
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	237
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October, 1998

III. Packaging Information

A. Package Type:	5-Pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0028
H. Flammability Rating:	Class UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: 	Level 1

IV. Die Information

A. Dimensions:	38 x 57 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord Bryan Preeshl (Manager, Reliability Operations) (Managing Director of QA)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{MTTF} = \underbrace{1.83}_{192 \text{ x } 4340 \text{ x } 80 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)} \\ \Box \\ \text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$

 $\lambda = 13.74 \times 10^{-9}$ $\lambda = 13.74$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5175) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.15 @ 25C and 2.60 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS12-1 die type has been found to have all pins able to withstand a transient pulse of \pm 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 100mA.

Table 1 Reliability Evaluation Test Results

MAX6504UKxx-T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23-5	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\frac{32}{2}$ No connects are not to be tested. $\frac{32}{2}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{RFF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of C. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





