RELIABILITY REPORT

FOR

MAX618EEE

PLASTIC ENCAPSULATED DEVICES

April 25, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager Reviewed by

Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MAX618 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Quality Assurance Information

VI.Reliability Evaluation

IV.Attachments

I. Device Description

A. General

The MAX618 CMOS, PWM, step-up DC-DC converter generates output voltages up to 28V and accepts inputs from +3V to +28V. An internal 2A, 0.3 switch eliminates the need for external power MOSFETs while supplying output currents up to 500mA or more. A PWM control scheme combined with Idle Mode^a operation at light loads minimizes noise and ripple while maximizing efficiency over a wide load range. No-load operating current is 500µA, which allows efficiency up to 93%.

A fast 250kHz switching frequency allows the use of small surface-mount inductors and capacitors. A shutdown mode extends battery life when the device is not in use. Adaptive slope compensation allows the MAX618 to accommodate a wide range of input and output voltages with a simple, single compensation capacitor.

The MAX618 is available in a thermally enhanced 16-pin QSOP package that is the same size as an industry-standard 8-pin SO but dissipates up to 1W. An evaluation kit (MAX618EVKIT) is available to help speed designs

B. Absolute Maximum Ratings

<u>ltem</u>	<u>Rating</u>
IN to GND	-0.3V to +30V
LX to VCC	-0.3V to +30V
VL to GND	-0.3V to +6V
/SHDN, COMP, FB to GND	-0.3V to (VL + 0.3V)
PGND to GND	+/-0.3V
Storage Temp.	+160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C) (Note 1)	
16-Pin QSOP	1W
Derates above +70°C	
16-Pin QSOP	15mW/°C

Note 1: With part mounted on 0.9in² of copper

II. Manufacturing Information

A. Description: 28V, PWM, Step-Up DC-DC Converters

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 1794

D. Fabrication Location: Oregon or California, USA

E. Assembly Location: Philippines or Korea

F. Date of Initial Production: April, 1999

III. Packaging Information

A. Package Type: 16-Lead QSOP

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (2.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1701-0347

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 85 x 145 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 160 \text{ x } 2}$$

$$\frac{1}{\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV$$

$$\lambda = 6.79 \text{ x } 10^{-9}$$

$$\lambda = 6.79 \text{ F.I.T. } (60\% \text{ confidence level @ 25°C})$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5382) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW99 die type has been found to have all pins able to withstand a transient pulse of ± 300 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA and/or ± 20 V.

Table 1Reliability Evaluation Test Results

MAX618EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

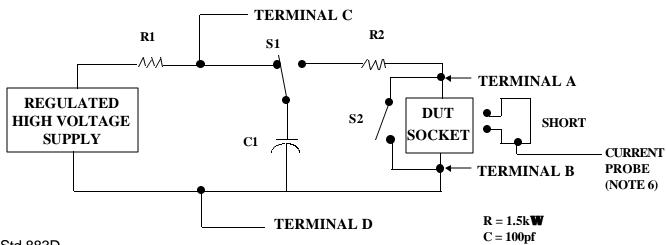
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2}$ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

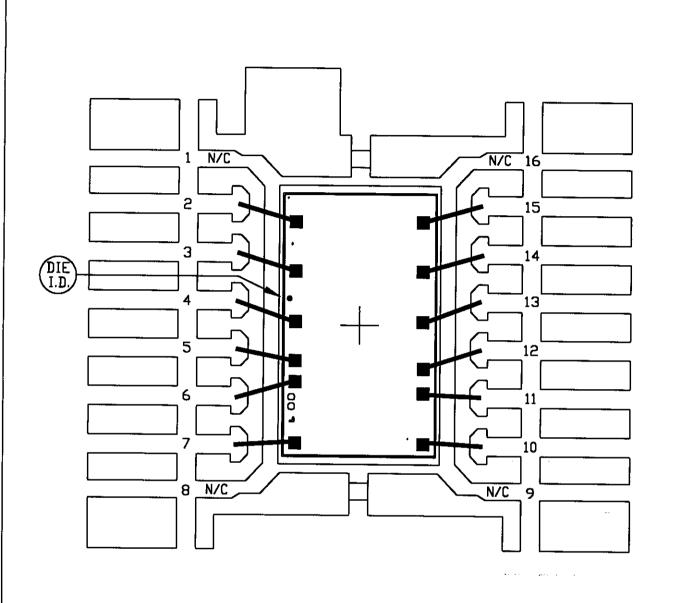
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{CC1} \), or \(\lambda_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG.CODE: E16-8F		APPROVALS	DATE	NIXI	/VI
CAV./PAD SIZE:	PKG,			BUILDSHEET NUMBER:	REV.:
101×154	DESIGN			05-1701-0347	A

