RELIABILITY REPORT

FOR

MAX5992AETG+T

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES

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Conclusion

The MAX5992AETG+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
.....Attachments
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX5992A–MAX5992C multisource, high-power, high-performance powered device (PD) controllers provide a complete interface control for PDs to comply with the IEEEM 802.3af/at standard in a Power-over- Ethernet (PoE) system. The devices provide the PD with a detection signature, classification signature, and an isolation MOSFET driver with current-limit control. In addition, the intelligent maintain power signature (MPS) and active FET bridge control make the PD more power efficient. The devices feature a SIG_OK output signal for high-power Multi-2P PD applications. The selectable inrush-current modes allow Multi-PD, fiber-to-the-home/ fiber-to-the-building (FTTH /FTTB) operation in redundancy applications. The devices feature an input UVLO, wide hysteresis, and long deglitch time to compensate for twisted-pair cable resistive drop to assure glitch-free transition during power-on /power-off conditions. The devices can operate from a 20.8V low-voltage supply by a selectable UVLO. The MAX5992C also supports 12V power adaptor to deliver power through a RJ45 connector without interfering with PoE detection/classification. The devices can withstand up to 80V at the input. The devices support a 2-Event classification method as specified in the IEEE 802.3at standard and provide a signal to indicate when probed by Type 2 power-sourcing equipment (PSE). The devices detect the presence of a wall adapter power-source connection and allow a smooth switchover from the PoE power source to the wall power adapter. Moreover, the selectable WAD_SEL supports seamless power transition from a wall adapter to PoE if PoE is already enabled. The devices also provide a power-good (PG) signal, 2-level current limit, foldback, and overtemperature protection. A sleep mode feature provides low-power consumption while supporting MPS. An ultra-low power sleep mode feature further reduces power consumption to comply with ultra-low power requirements while still supporting MPS. The devices also feature an LED driver that is automatically activated during sleep/ultra-low power sleep/MPS mode. The MAX5992A has 38.6V PoE UVLO and the MAX5992B/MAX5992C have 35.4V PoE UVLO and feature a 6.5s sleep mode delay. The MAX5992A–MAX5992C are available in a 24-pin, 4mm x 4mm, TQFN power package and are rated over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Multisource, High-Power, High-Performance Powered Device Controllers
B. Process:	S18
C. Number of Device Transistors:	13282
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	September 29, 2012

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (1 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-5005
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	48°C/W
J. Single Layer Theta Jc:	2.7°C/W
K. Multi Layer Theta Ja:	36°C/W
L. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	64.5669X65.3543 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 139 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.91 \times 10^{-9}$

$\lambda = 7.91$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The NQ84-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78

With the following exception:

WAD pin passes +100mA/-50mA per JEDEC JESD78
DET pin passes +100mA/-90mA per JEDEC JESD78
SIGOKB pin passes +100mA/-70mA per JEDEC JESD78
VIN1 pin passes +100mA/-90mA per JEDEC JESD78

Table 1

Reliability Evaluation Test Results

MAX5992AETG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	139	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.