RELIABILITY REPORT

FOR

MAX5946xETX

PLASTIC ENCAPSULATED DEVICES

June 14, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Conclusion

The MAX5946 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. ....Device Description
II. ....Manufacturing Information
III. ....Packaging Information
.....Attachments
V. ....Quality Assurance Information
VI. ....Reliability Evaluation
IV. ....Die Information

I. Device Description

A. General

The MAX5946 dual hot-plug controller is designed for PCI Express™ applications. The device provides hotplug control for 12V, 3.3V, and 3.3V auxiliary supplies of two PCI express slots. The MAX5946's logic inputs/outputs allow interfacing directly with the system hot-plug management controller or through an SMBus™ with an external I/O expander. An integrated debounced attention switch and present-detect signals are included to simplify system design.

The MAX5946 drives four external n-channel MOSFETs to control the 12V and 3.3V main outputs. The 3.3V auxiliary outputs are controlled through internal 0.3Ω n-channel MOSFETs. Internal charge pumps provide gate drive for the 12V outputs while the gate drive of the 3.3V output is driven by the 12V input supply. The 3.3V auxiliary outputs are completely independent from the main outputs with their own charge pumps.

At power-up, the MAX5946 keeps all of the external MOSFETs off until the supplies rise above their respective undervoltage lockout (UVLO) thresholds. The device keeps the internal MOSFETs off only until the auxiliary input supply rises above its UVLO threshold. Upon a turn-on command, the MAX5946 enhances the external and internal MOSFETs slowly with a constant gate current to limit the power-supply inrush current. The MAX5946 actively limits the current of all outputs at all times and shuts down if an overcurrent condition persists for longer than a programmable overcurrent timeout. Thermal-protection circuitry also shuts down all outputs if the die temperature exceeds +150°C. After an overcurrent or overtemperature fault condition, the MAX5946L latches off while the MAX5946A automatically restarts after a restart time delay. The device is available in a 36-pin (6mm °— 6mm) thin QFN package and operates over the -40°C to +85°C temperature range

B. Absolute Maximum Ratings

Item	Rating
12VIN	-0.3V to +14V
12GA, 12GB	-0.3V to (V12VIN + 6V)
12SA+, 12SA-, 12SB+, 12SB-,	
3.3GA, 3.3GB	-0.3V to (V12VIN + 0.3V)
3.3VAUXIN, ONA, ONB, FAULTA, FAULTB	-0.3V to +6V
PWRGDA, PWRGDB	-0.3V to +6V
PGND	-0.3V to +0.3V
All Other Pins to GND	-0.3V to (V3.3VAUXIN + 0.3V)
Continuous Power Dissipation (TA = +70°C)	
36-Pin Thin QFN (derate 26.3mW/°C above +70°C)	2.105W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: *Dual PCI Express, Hot-Plug Controller*

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 10,487

D. Fabrication Location: California, USA

E. Assembly Location: Thailand

F. Date of Initial Production: November, 2004

III. Packaging Information

A. Package Type: **36-Pin TQFN**

B. Lead Frame: Copper

C. Lead Finish: Solder-Plate or100% Matte Tin

D. Die Attach: Silver Filled Epoxy

E. Bondwire: Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-1292

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

A. Dimensions: 113 x 105 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.71 \times 10^{-9}$

λ = 13.71 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-6374) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP74Z die type has been found to have all pins able to withstand a transient pulse of ±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX5946xETX

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

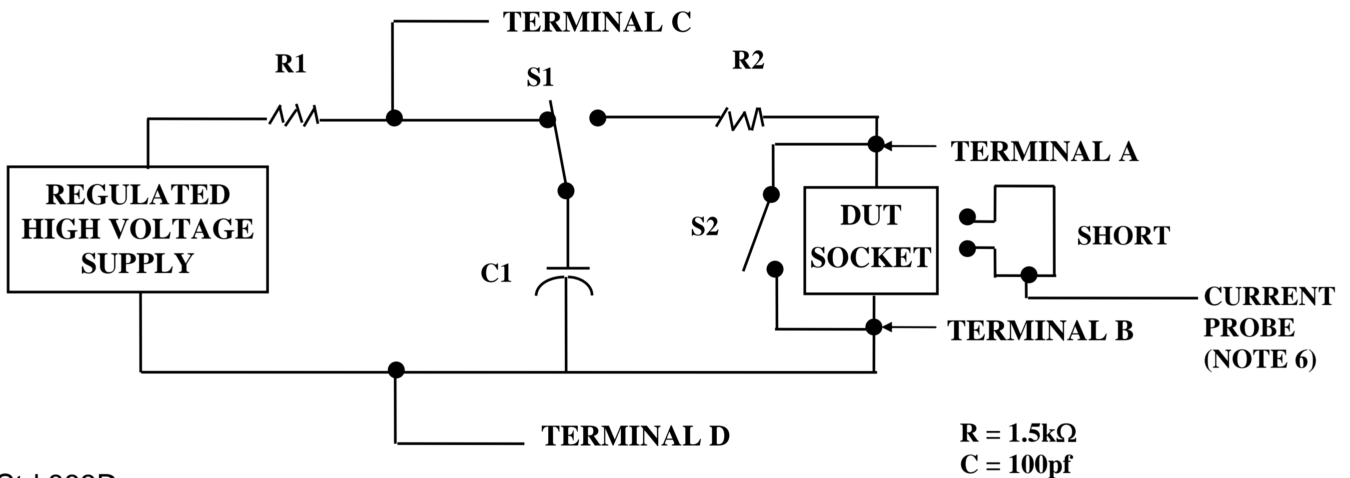
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

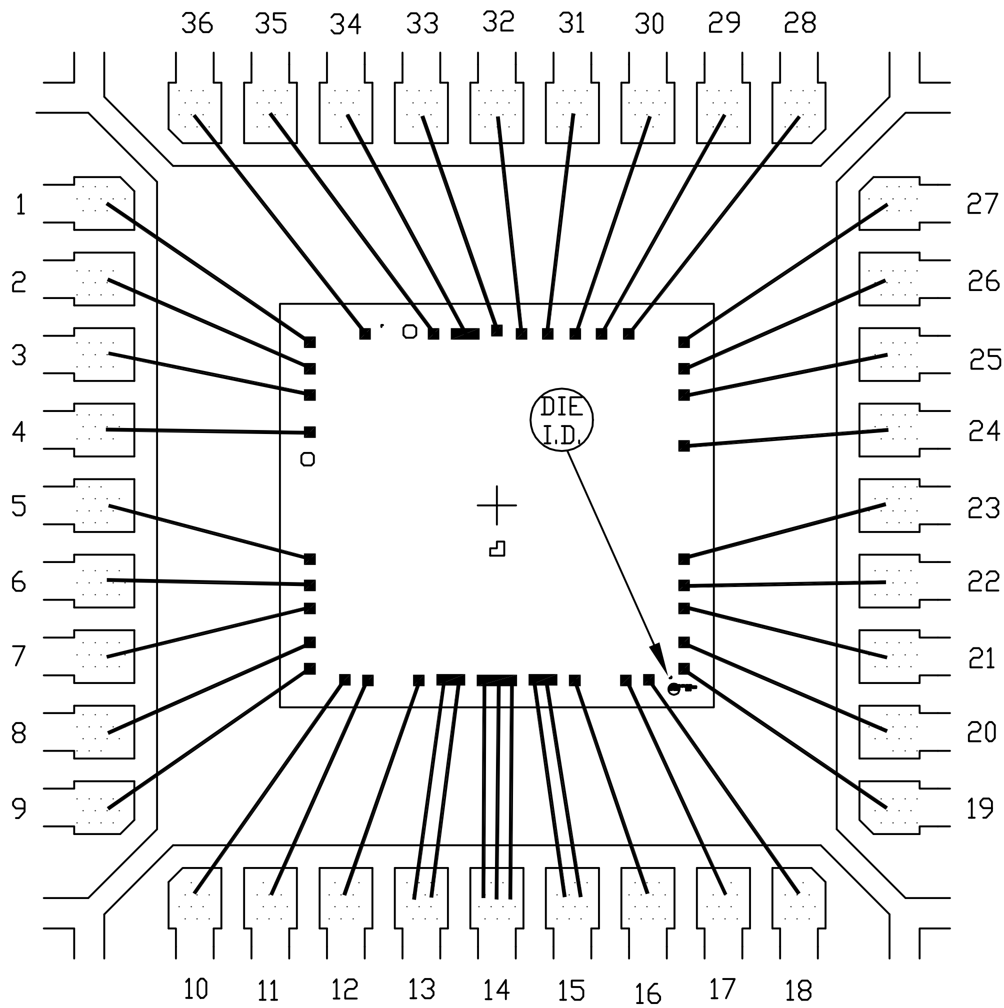
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

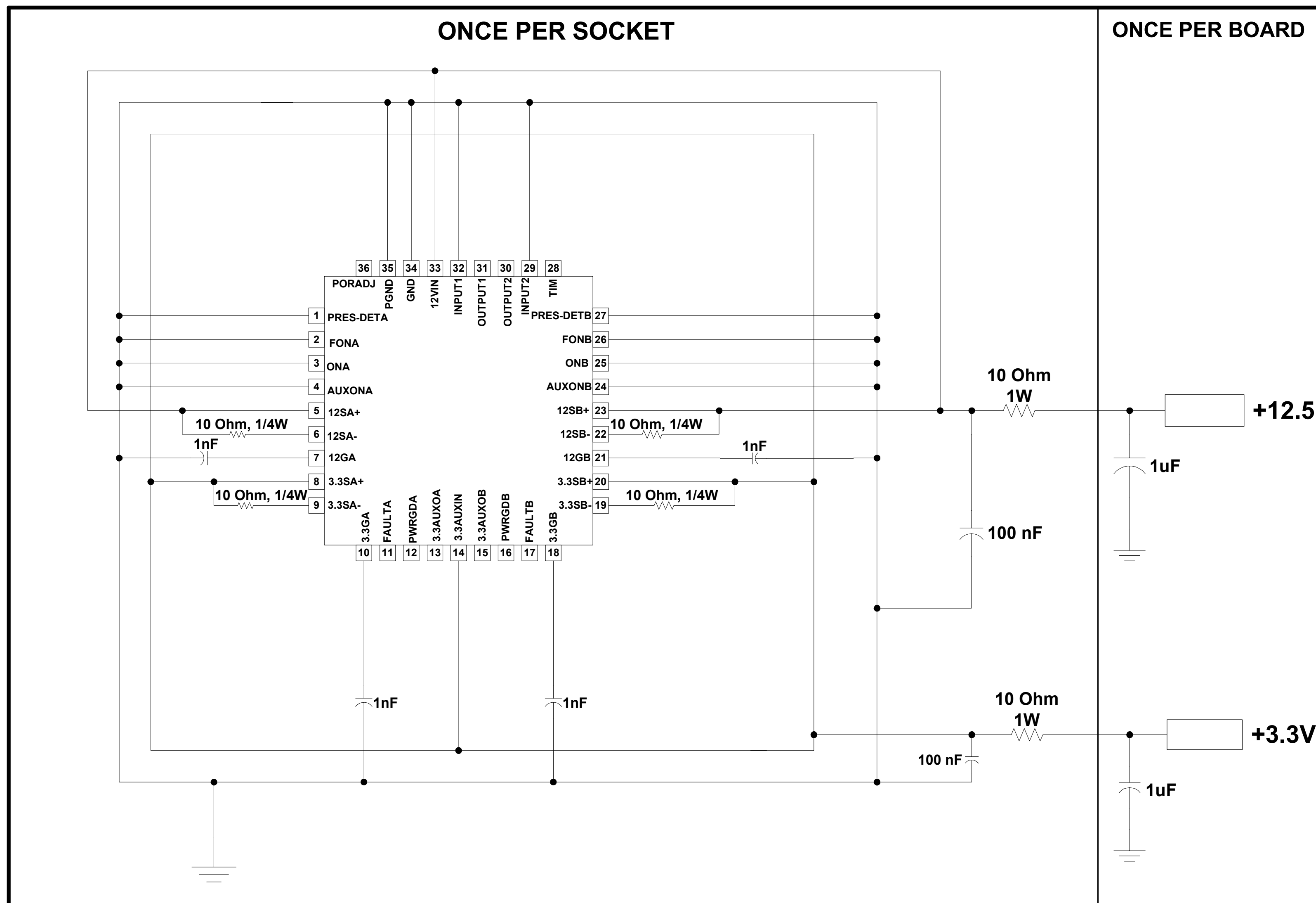


6x6x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.



PKG. CODE: T3666-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 177x177	PKG.			BOND DIAGRAM #: 05-9000-1292	REV: A
	DESIGN				



DEVICES: MAX5946 (NP74Z)
PACKAGE: 36-QFN 6x6 THIN
MAX Expected current : 1mA (+12.5V), 4mA (+3.3V)

NOTES: TYPICAL CURRENT = 0.5mA (+12.5V), 2mA (+3.3V)

DOCUMENT I.D. 06-6376	REVISION A	*MAXIM* TITLE: BI Circuit: MAX5946 (NP74Z)	PAGE 2