RELIABILITY REPORT

FOR

MAX5478Exx

PLASTIC ENCAPSULATED DEVICES

May 15, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX5478 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5478 nonvolatile, dual, linear-taper, digital potentiometers perform the function of a mechanical potentiometer, but replace the mechanics with a simple 2-wire digital interface. Each device performs the same function as a discrete potentiometer or variable resistor and has 256 tap points.

The devices feature an internal, nonvolatile EEPROM used to store the wiper position for initialization during power-up. A write-protect feature prevents accidental overwrites of the EEPROM. The fast-mode I^2C*-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnection complexity in many applications. Three address inputs allow a total of eight unique address combinations.

The MAX5478 provides a nominal resistance values of 50kΩ. The nominal resistor temperature coefficient is 35ppm/°C end-to-end and 5ppm/°C ratiometric. The low temperature coefficient makes the devices ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain-amplifier circuit configurations.

The MAX5478 is available in 16-pin 3mm x 3mm x 0.8mm thin QFN and 14-pin 4.4mm x 5mm TSSOP packages. These devices operate over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
SDA, SCL, VDD to GND	-0.3V to +6.0V
All Other Pins to GND	-0.3V to (VDD + 0.3V)
Maximum Continuous Current into H_, L_, and W_	±1.3mA
Continuous Power Dissipation (TA = +70°C)	
16-Pin Thin QFN (derate 17.5mW/°C above +70°C)	1398mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Dual, 256-Tap, Nonvolatile, I2C-Interface, Digital Potentiometers
B. Process:	D35/E35
C. Number of Device Transistors:	12,651
D. Fabrication Location:	Texas, USA
E. Assembly Location:	Thailand, Malaysia, or Philippines
F. Date of Initial Production:	July, 2004

III. Packaging Information

A. Package Type:	**16-Pin TDFN (3x3)**	**14-Pin TSSOP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate or 100% Matte Tin
D. Die Attach:	N/A	Silver-Filled Epoxy
E. Bondwire:	N/A	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1170	# 05-9000-1178
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	94 x 91 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.45 microns, Metal2 = 0.5 microns, Metal3 = 0.6 (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns, Metal2 = 0.5 microns, Metal3 = 0.6 (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.91 \times 10^{-9}$

λ = 22.91 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6360) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the D35/E35 Process results in a FIT Rate of 0.34 @ 25C and 5.69 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DP20-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

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Table 1
Reliability Evaluation Test Results

MAX5478Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFN TSSOP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

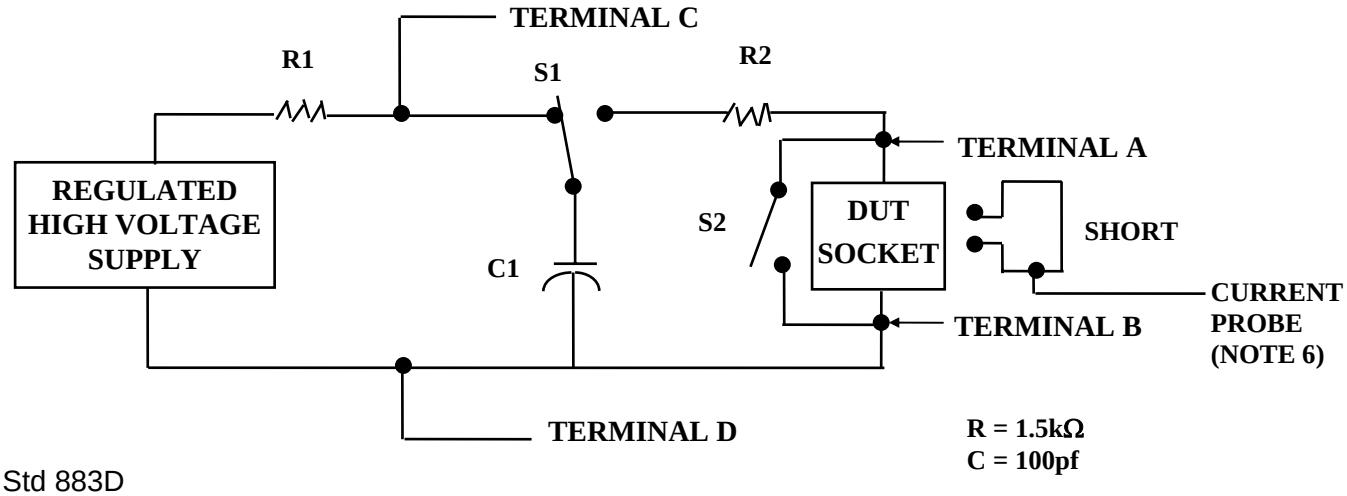
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

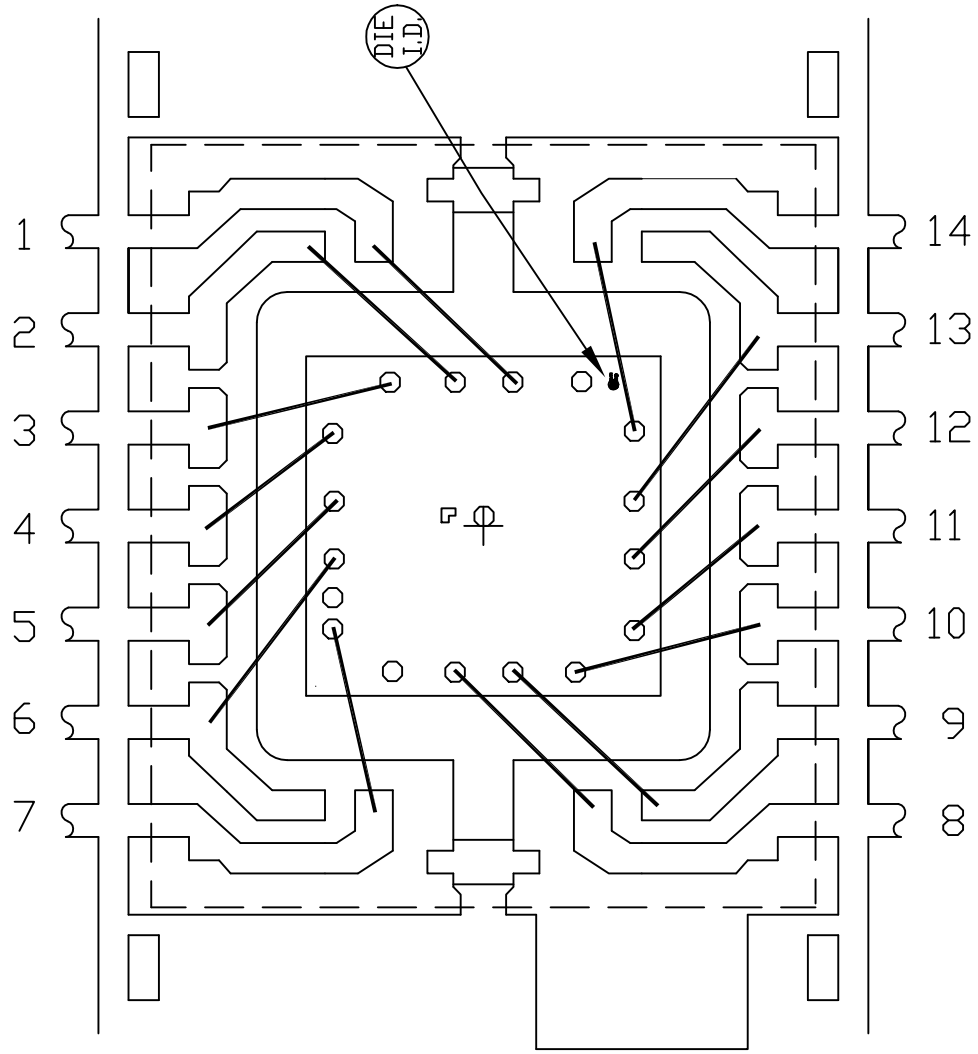
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

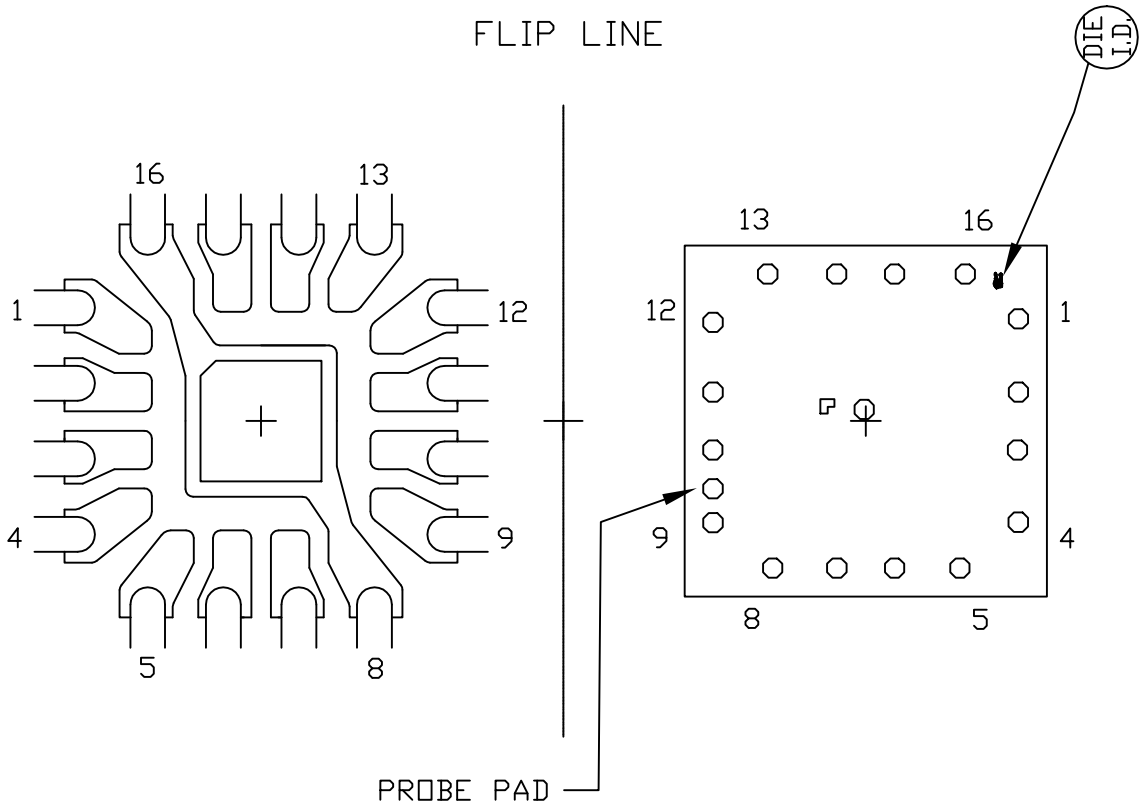
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



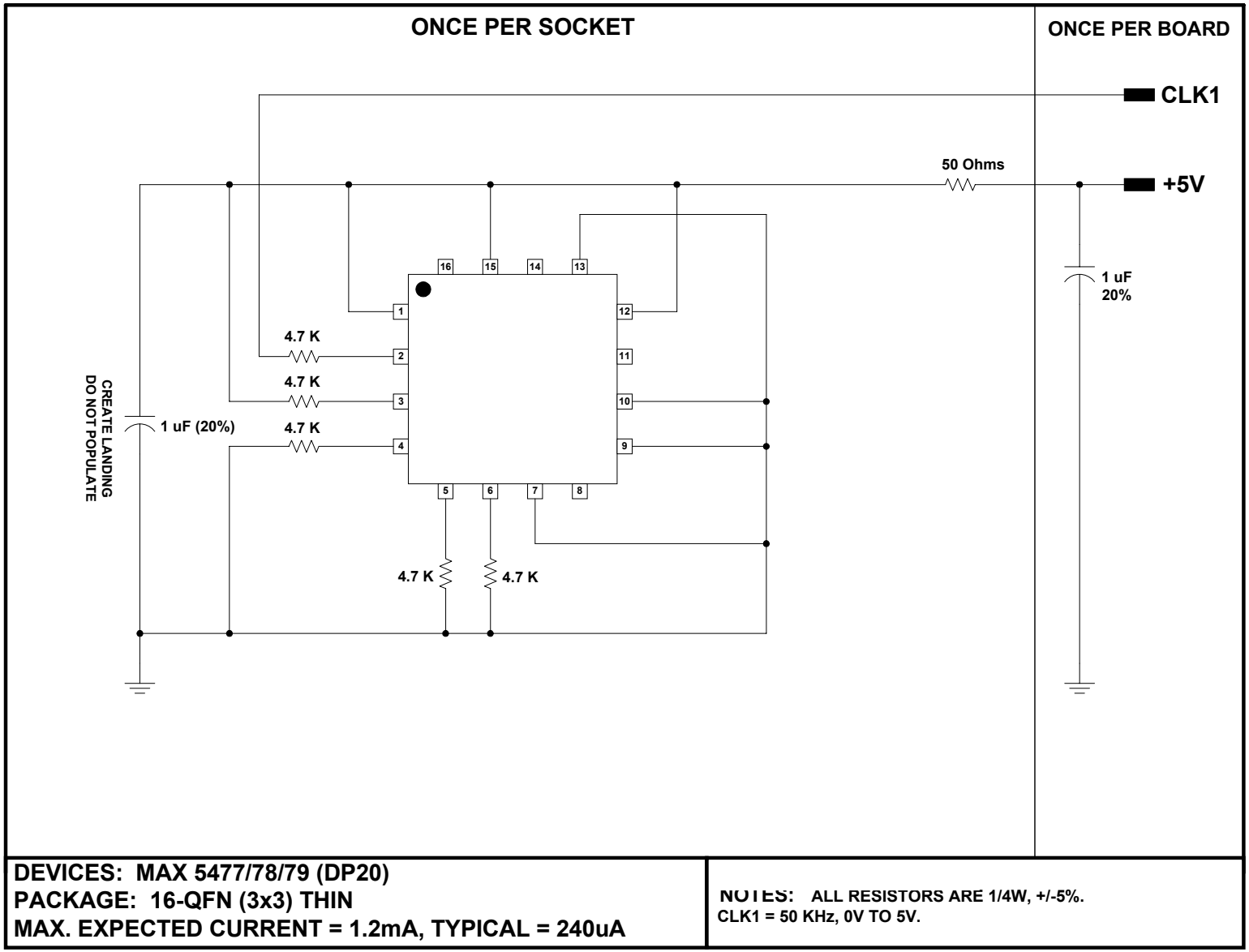


PKG. CODE: U14-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118×122	PKG.			BOND DIAGRAM #: 05-9000-1178	REV: A
	DESIGN				

3x3x0.8mm QFN THIN PKG.
FLIP CHIP
WITH EXPOSED PAD



PKG. CODE: T1633F-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG.			BOND DIAGRAM #: 05-9000-1170	REV: A
	DESIGN				



DEVICES: MAX 5477/78/79 (DP20)
PACKAGE: 16-QFN (3x3) THIN
MAX. EXPECTED CURRENT = 1.2mA, TYPICAL = 240uA

NOTES: ALL RESISTORS ARE 1/4W, +/-5%.
CLK1 = 50 KHz, 0V TO 5V.