RELIABILITY REPORT

FOR

MAX530xxxG

PLASTIC ENCAPSULATED DEVICES

April 15, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX530 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX530 is a low-power, 12-bit, voltage-output digital-to-analog converter (DAC) that uses single +5V or dual ±5V supplies. This device has an on-chip voltage reference plus an output buffer amplifier. Operating current is only 250µA from a single +5V supply, making it ideal for portable and battery-powered applications. In addition, the SSOP (Shrink-Small-Outline-Package) measures only 0.1 square inches, using less board area than an 8-pin DIP. 12-bit resolution is achieved through laser trimming of the DAC, op amp, and reference. No further adjustments are necessary.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or ±2.048V. Four-quadrant multiplication is possible without the use of external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-bit, 8-bit, and 16-bit microprocessors. For DACs with similar features but with a serial data interface, refer to the MAX531/MAX538/MAX539 data sheet.

B. Absolute Maximum Ratings

Item	Rating
VDD to DGND and VDD to AGND	-0.3V, +6V
VSS to DGND and VSS to AGND	-6V, +0.3V
VDD to VSS	-0.3V, +12V
AGND to DGND	-0.3V, +0.3V
REFGND to AGND	-0.3V, (VDD + 0.3V)
Digital Input Voltage to DGND	-0.3V, (VDD + 0.3V)
REFIN	(VSS - 0.3V), (VDD + 0.3V)
REFOUT	(VSS - 0.3V), (VDD + 0.3V)
REFOUT to REFGND	-0.3V, (VDD + 0.3V)
RFB	(VSS - 0.3V), (VDD + 0.3V)
ROFS	(VSS - 0.3V), (VDD + 0.3V)
Continuous Current, Any Input	±20mA
Operating Temperature Ranges:	
MAX530_C_ _	0°C to +70°C
MAX530_E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation	
24-Lead Plastic NDIP	1067mW
24-Lead WSO	941mW
24-Lead SSOP	640mW
Derates above +70°C	
24-Lead Plastic DIP	13.33mW/°C
24-Lead WSO	11.76mW/°C
24-Lead SSOP	8.00mW/°C

Note 1: The output may be shorted to VDD, VSS, DGND, or AGND if the continuous package power dissipation and current ratings are not exceeded. Typical short-circuit currents are 20mA.

II. Manufacturing Information

A. Description/Function:	+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	913
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	December, 1993

III. Packaging Information

A. Package Type:	**24-Pin PDIP**	**24-Pin WSO**	**24-Pin SSOP**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0370	# 05-0401-0371	# 05-0401-0372
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	87 x 133 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 400 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 5.99 \times 10^{-9}$

$\lambda = 5.99$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0122) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DA45 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX530xxxG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		400	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP SO uMAX	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

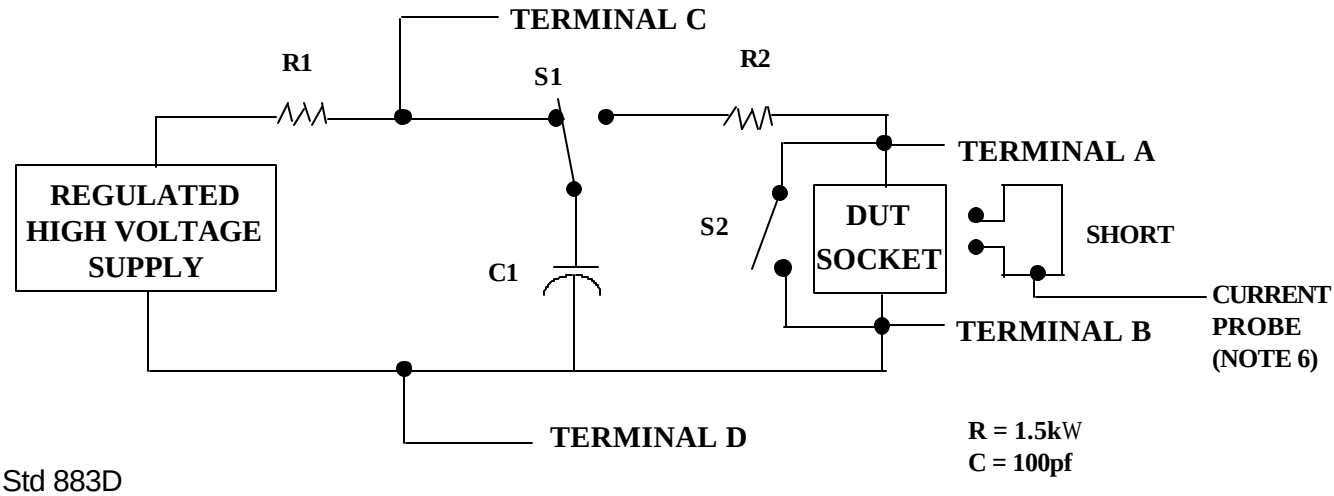
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

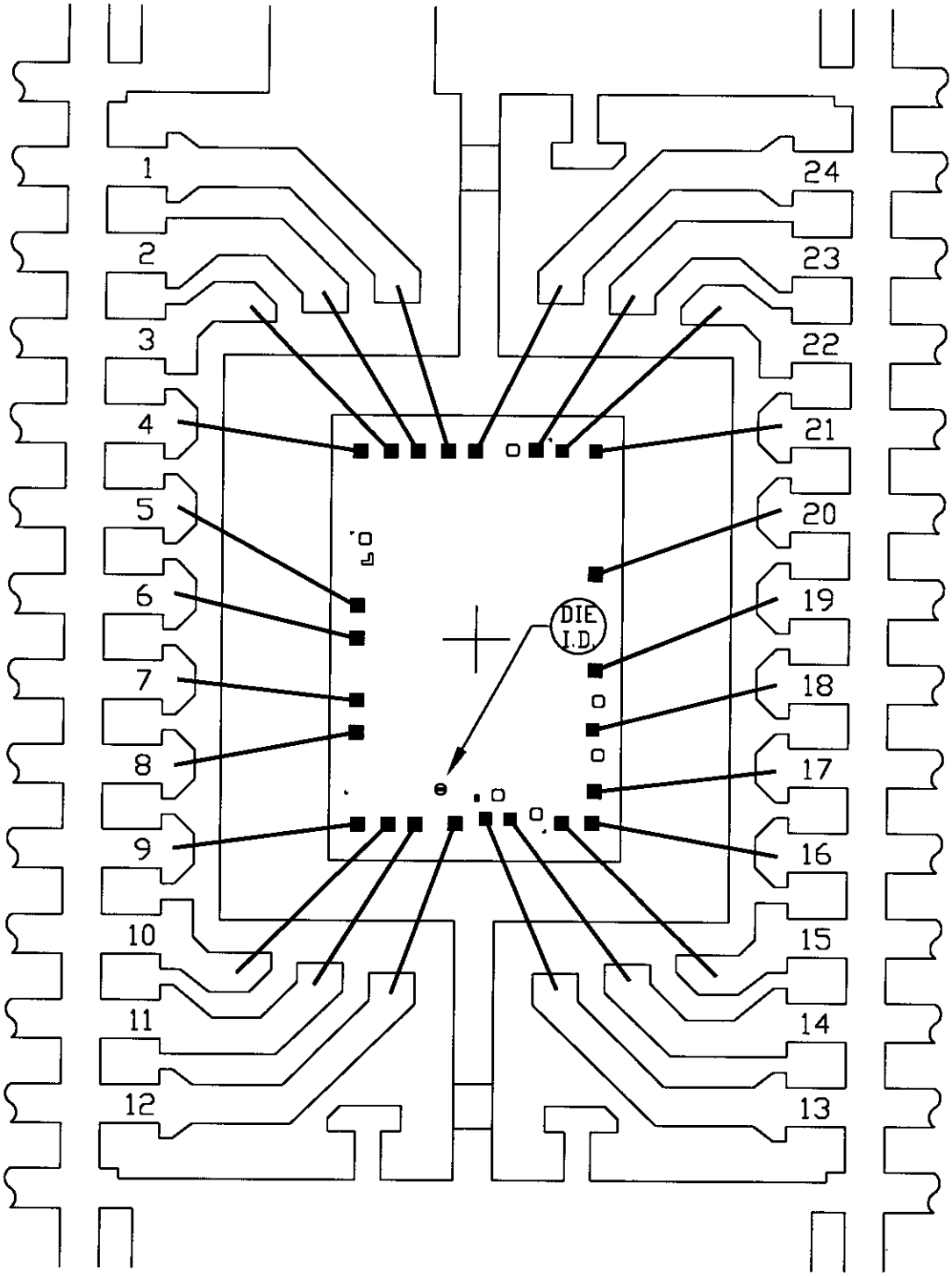
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

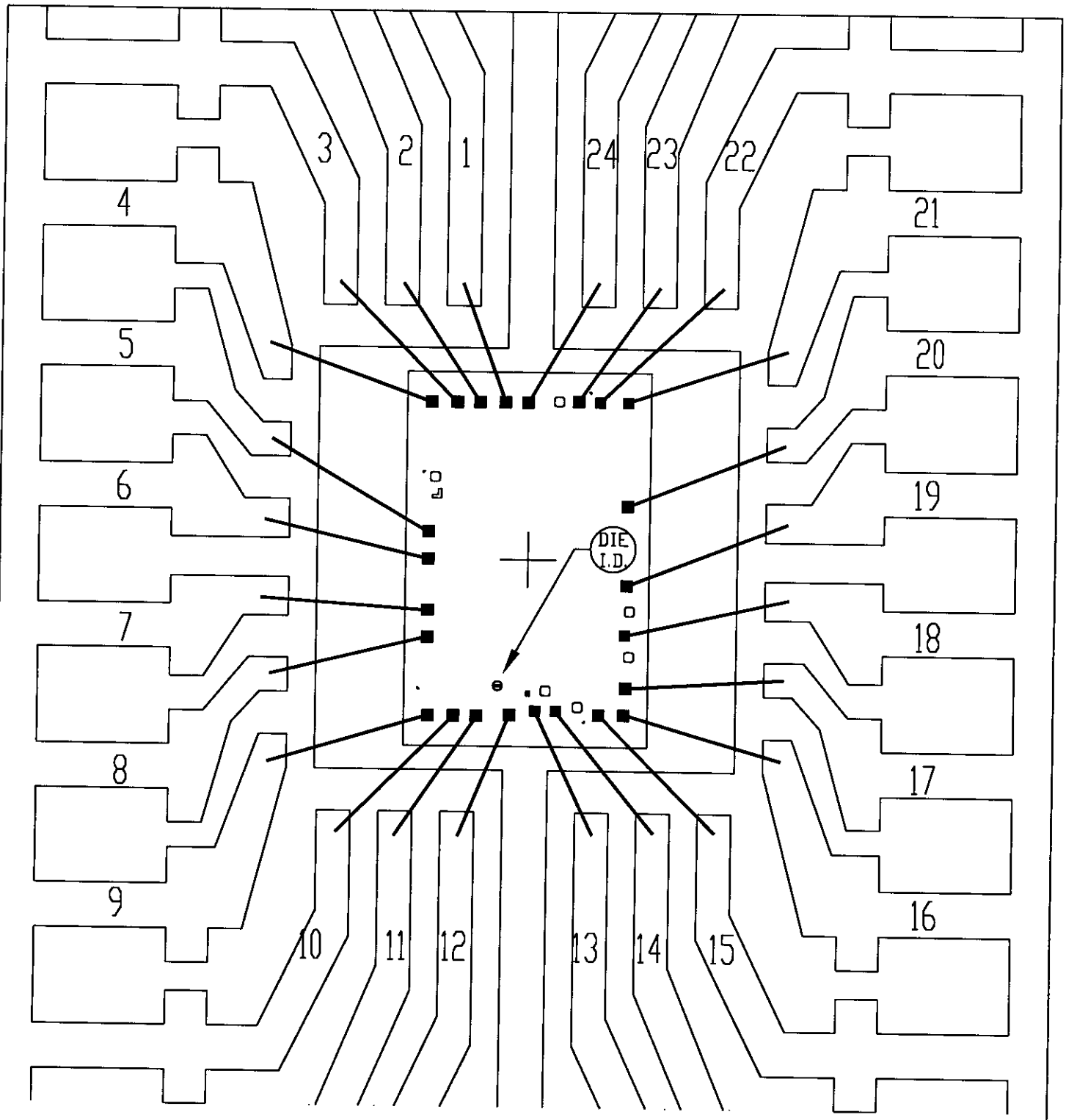
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



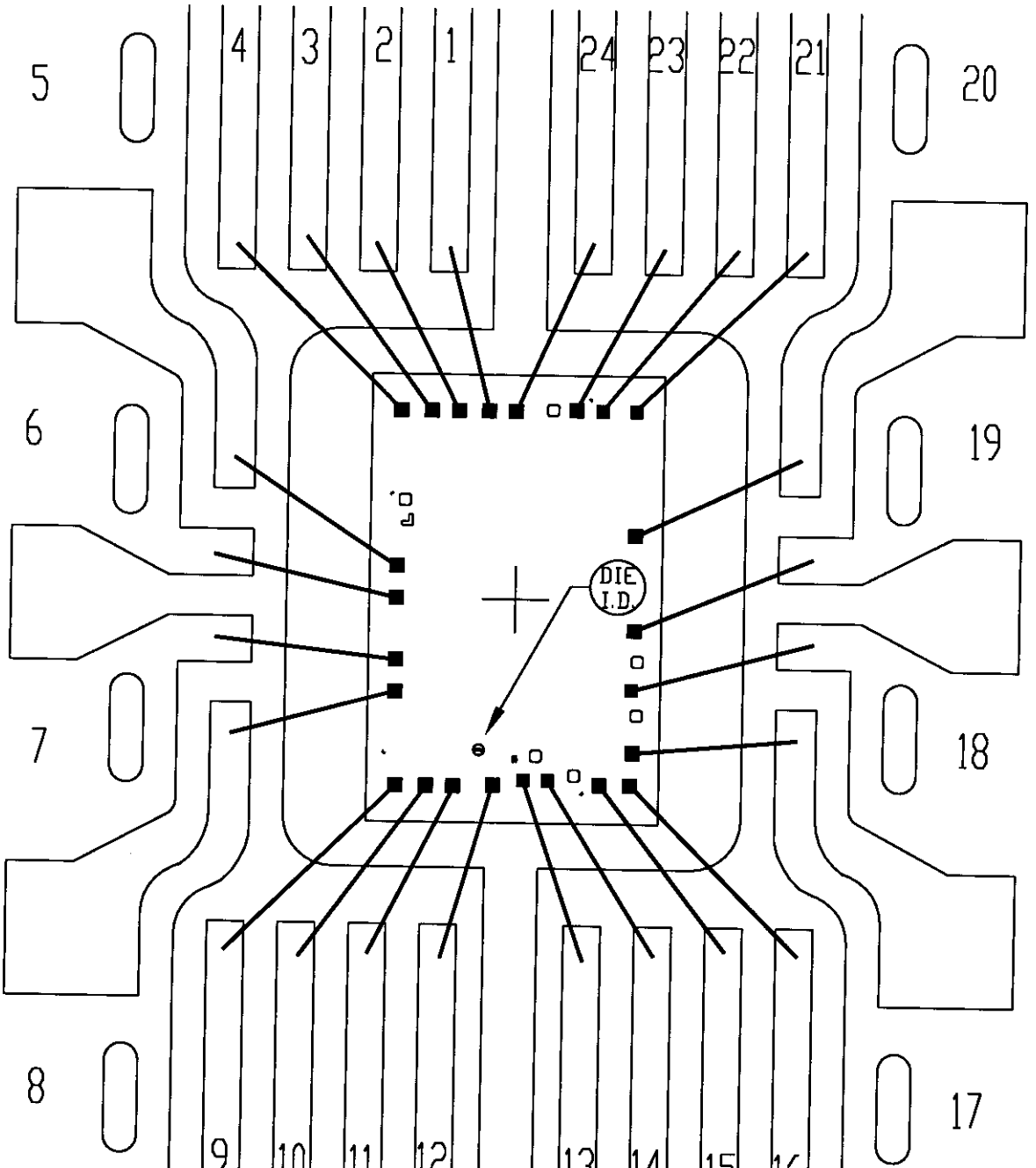
Mil Std 883D
Method 3015.7
Notice 8



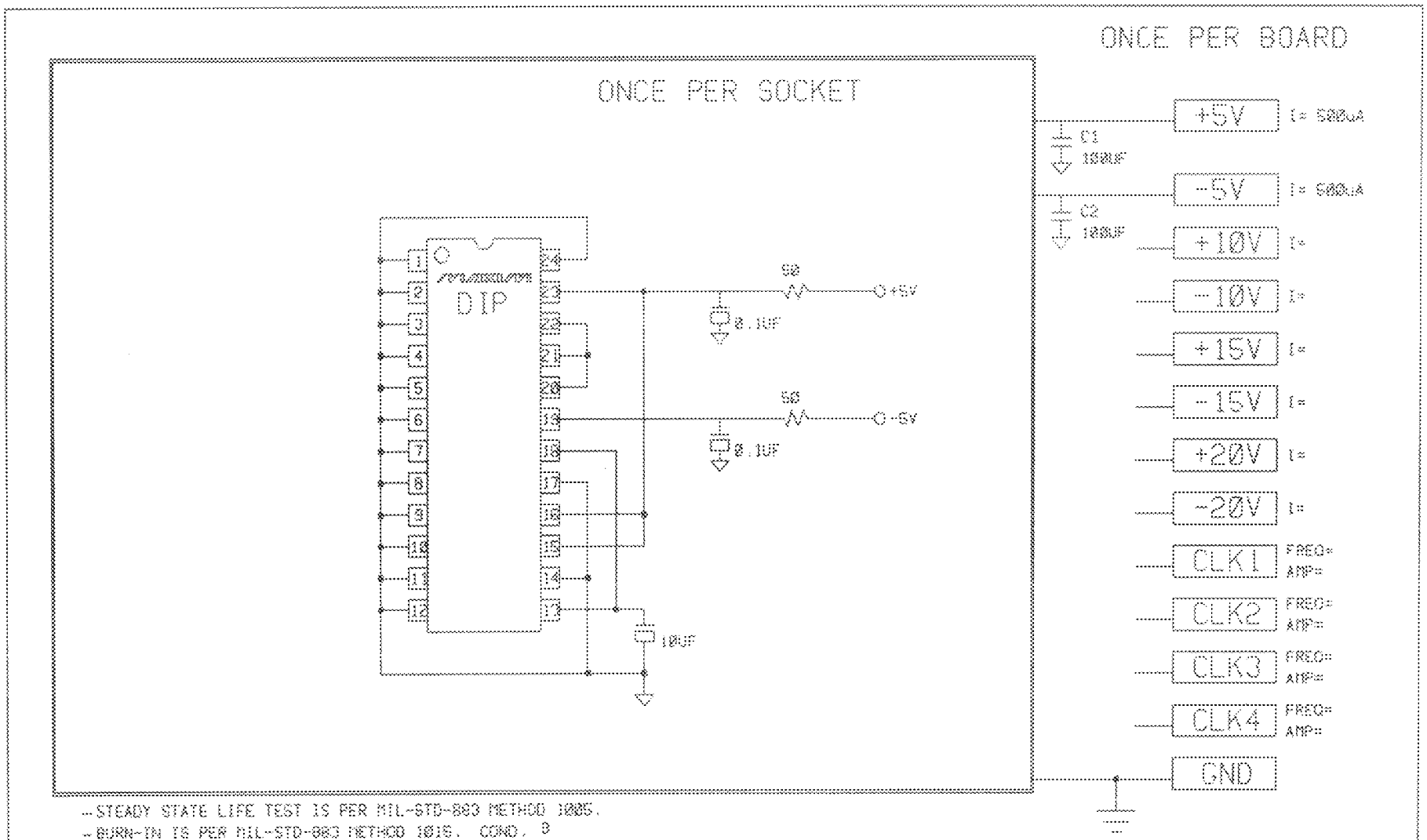
PKG. CODE: A24-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 154X169	PKG. DESIGN			BOND DIAGRAM #: 05-0401-0372 / REV: B



PKG. CODE: W24-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 150 X 150	PKG. DESIGN			BOND DIAGRAM #: 05-0401-0371 REV: B



PKG. CODE: N24-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 136 X 160	PKG. DESIGN			BOND DIAGRAM #: 05-0401-0370 REV: B



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR EXT COMMERCIAL
   EXT MR/883

SPEC. NO. 06-0122 REV. B

DATE: 8/1/94

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX503/530