RELIABILITY REPORT

FOR

MAX5215GUA+

PLASTIC ENCAPSULATED DEVICES

August 22, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX5215GUA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5215/MAX5217 are pin-compatible 14-bit and 16-bit digital-to-analog converters (DACs). The MAX5215/MAX5217 are single-channel, low-powered, buffered voltage-output DACs. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption. The MAX5215/MAX5217 accept a wide 2.7V to 5.5V supply voltage range. Power consumption is extremely low to accommodate most low-power and low-voltage applications. The MAX5215/MAX5217 have an I²C-compatible, 2-wire serial interface that operates at clock rates up to 400kHz. On power-up, the MAX5215/MAX5217 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers that need to be off on power-up. The DAC output is buffered resulting in a low supply current of 80µA (max) and a low offset error of ±0.25mV. An asynchronous active-low input, AUX, is provided. This input can be programmed to support clear or load DAC operations, independent of the serial interface. The MAX5215/MAX5217 are available in an ultra-small (3mm x 5mm), 8-pin µMAX® package and are specified over the -40°C to +105°C extended industrial temperature range.

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II. Manufacturing Information

A. Description/Function:	14-/16-Bit, Low-Power, Buffered Rail-to-Rail DACs with I²C Interface
B. Process:	S45
C. Number of Device Transistors:	34312
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	November 30, 2012

III. Packaging Information

A. Package Type:	3x3mm 8L UMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4890
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	42°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	42°C/W

IV. Die Information

A. Dimensions:	66X88 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot TACX9Q001B, D/C 1205)

The DB55-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX5215GUA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	TACX9Q001A, D/C 1205

Note 1: Life Test Data may represent plastic DIP qualification lots.

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