

RELIABILITY REPORT
FOR
MAX5135GTG+
PLASTIC ENCAPSULATED DEVICES

February 26, 2009

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX5135GTG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5134-MAX5137 is a family of pin-compatible and software-compatible 16-bit and 12-bit DACs. The MAX5134/MAX5135 are low-power, quad 16-/12-bit, buffered voltage-output, high-linearity DACs. The MAX5136/MAX5137 are low-power, dual 16-/12-bit, buffered voltage-output, high-linearity DACs. They use a precision internal reference or a precision external reference for rail-to-rail operation. The MAX5134-MAX5137 accept a wide +2.7V to +5.25V supply-voltage range to accommodate most low-power and low-voltage applications. These devices accept a 3-wire SPI(tm)/QSPI(tm)/MICROWIRE(tm)/DSP-compatible serial interface to save board space and reduce the complexity of optically isolated and transformer-isolated applications. The digital interface's double-buffered hardware and software active-low LDAC provide simultaneous output updates. The serial interface features an active-low READY output for easy daisy-chaining of several MAX5134-MAX5137 devices and/or other compatible devices. The MAX5134-MAX5137 include a hardware input to reset the DAC outputs to zero or midscale upon power-up or reset, providing additional safety for applications that drive valves or other transducers that need to be off during power-up. The high linearity of the DACs makes these devices ideal for precision control and instrumentation applications. The MAX5134-MAX5137 are available in an ultra-small (4mm x 4mm), 24-pin TQFN package and are specified over the -40°C to +105°C extended industrial temperature range.

II. Manufacturing Information

A. Description/Function:	Pin-/Software-Compatible, 16-/12-Bit, Voltage-Output DACs
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	ASAT China, UTL Thailand, Unisem Malaysia, ISPL Philippines
F. Date of Initial Production:	October 20, 2008

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	97 X 97 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DB34 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX5135GTG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data