RELIABILITY REPORT

FOR

MAX5105EEP+
(MAX5105 – MAX5106)

PLASTIC ENCAPSULATED DEVICES

December 16, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX5105EEP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX5105/MAX5106 nonvolatile, quad, 8-bit digital-to-analog converters (DACs) operate from a single +2.7V to +5.5V supply. An internal EEPROM stores the DAC states even after power is removed. Data from these nonvolatile registers automatically initialize the DAC outputs and operating states during power-up. Precision internal buffers swing rail-to-rail, and the reference input range includes both ground and the positive rail. The MAX5105/MAX5106 feature a software-controlled 10µA shutdown mode and a mute state that drives the DAC outputs to their respective REFL_ voltages. The MAX5105 includes an asynchronous MUTE input, as well as a RDY/BSY-bar output that indicates the status of the nonvolatile memory. The MAX5105 is available in 20-pin QSOP and 20-pin wide SO packages, and the MAX5106 is available in a 16-pin QSOP package.

II. Manufacturing Information

A. Description/Function:	Nonvolatile, Quad, 8-Bit DACs
B. Process:	TSMC 0.5µm Silicon Gate CMOS
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Stats Singapore, ATP Philippines, UTL Thailand
F. Date of Initial Production:	January 23, 2001

III. Packaging Information

A. Package Type:	20-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0542
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	34°C/W
L. Multi Layer Theta Ja:	90.5°C/W
M. Multi Layer Theta Jc:	34°C/W

IV. Die Information

A. Dimensions:	84 X 128 mils
B. Passivation:	SiO_2 (Oxide)/Si_3N_4 (Nitride)
C. Interconnect:	Al/Cu (0.5%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.5um
F. Minimum Metal Spacing:	0.5um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon dioxide
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are complete. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.4 \times 10^{-9}$

λ = 13.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TSMC 0.5um Process results in a FIT Rate of 4.5 @ 25C and 77.5 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DA87 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX5105EEP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data