

RELIABILITY REPORT
FOR
MAX5104xEE
PLASTIC ENCAPSULATED DEVICES

October 23, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX5104 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5104 low-power, serial, voltage-output, dual 12-bit digital-to-analog converter (DAC) consumes only 500 μ A from a single +5V supply. This device features Rail-to-Rail[®] output swing and is available in a space-saving 16-pin QSOP package. To maximize the dynamic range, the DAC output amplifiers are configured with an internal gain of +2V/V.

The 3-wire serial interface is SPI[™]/QSPI[™]/MICROWIRE[™] compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include programmable power-down (2 μ A), hardware power-down lockout (PDL), a separate reference voltage input for each DAC that accepts AC and DC signals, and an active-low clear input (CL) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality, and a serial-data output pin for daisy chaining.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD to AGND	-0.3V to +6V
VDD to DGND	-0.3V to +6V
AGND to DGND	\pm 0.3V
OSA, OSB to AGND	VAGND - 4V) to (VDD + 0.3V)
REF_, OUT_ to AGND	-0.3V to (VDD + 0.3V)
Digital Inputs (SCLK, DIN, CS, CL, PDL) to DGND	(-0.3V to +6V)
Digital Outputs (DOUT, UPO) to DGND	-0.3V to (VDD + 0.3V)
Maximum Current into Any Pin	\pm 20mA
Operating Temperature Ranges	
MAX5104CEE	0°C to +70°C
MAX5104EEE	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	3053
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Thailand
F. Date of Initial Production:	November, 1999

III. Packaging Information

A. Package Type:	16-Lead QSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0401-0493
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	86 x 114 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 14.98 \times 10^{-9} \quad \lambda = 14.98 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5269) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA65-2 die type has been found to have all pins able to withstand a transient pulse of ± 2000 , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1
Reliability Evaluation Test Results

MAX5104xEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

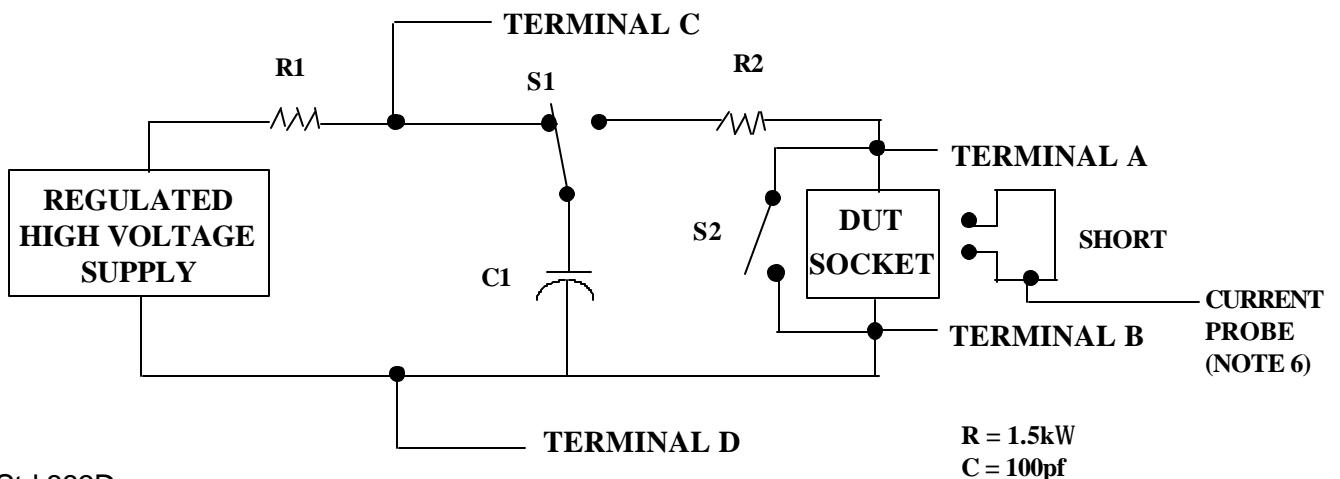
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

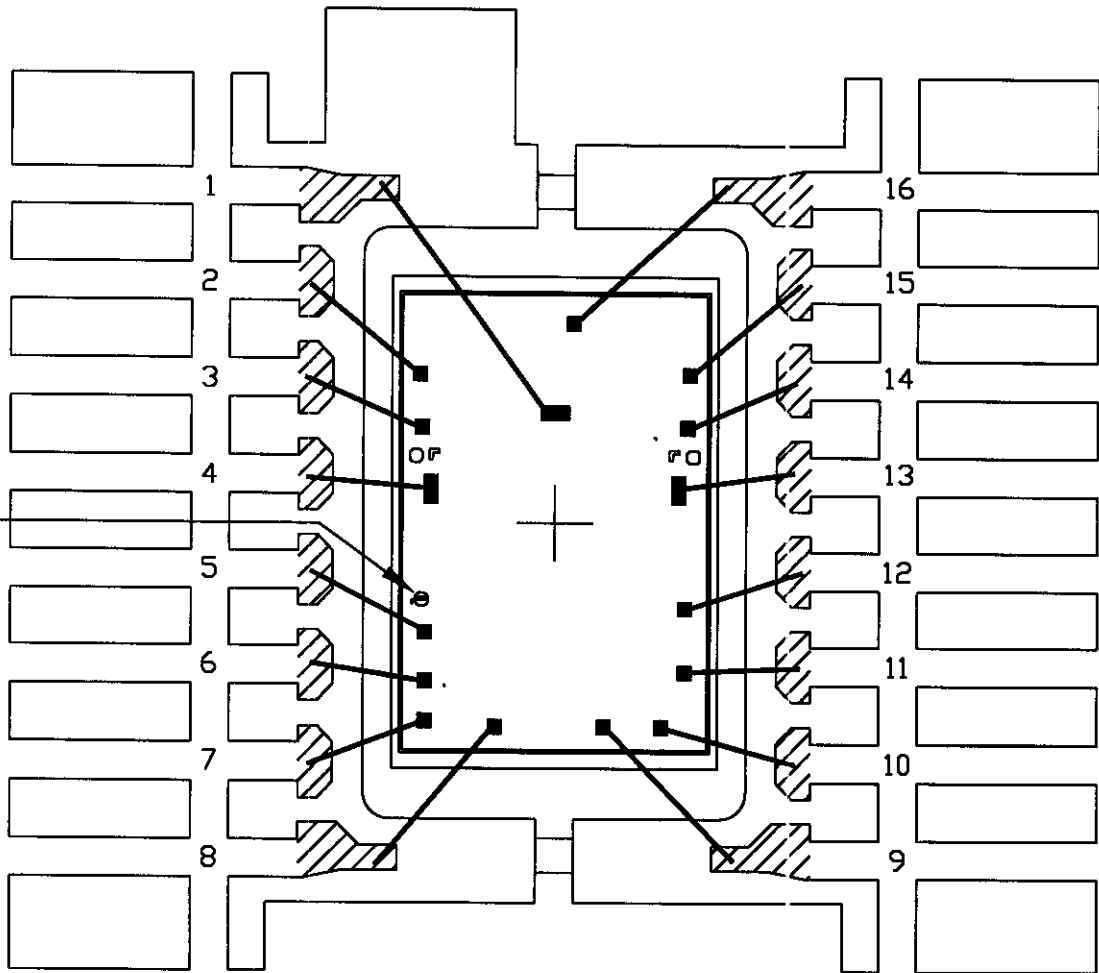
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



DIE
I.D.



PKG.CODE: E16-5

CAV./PAD SIZE:
101x154

PKG.
DESIGN

APPROVALS

DATE

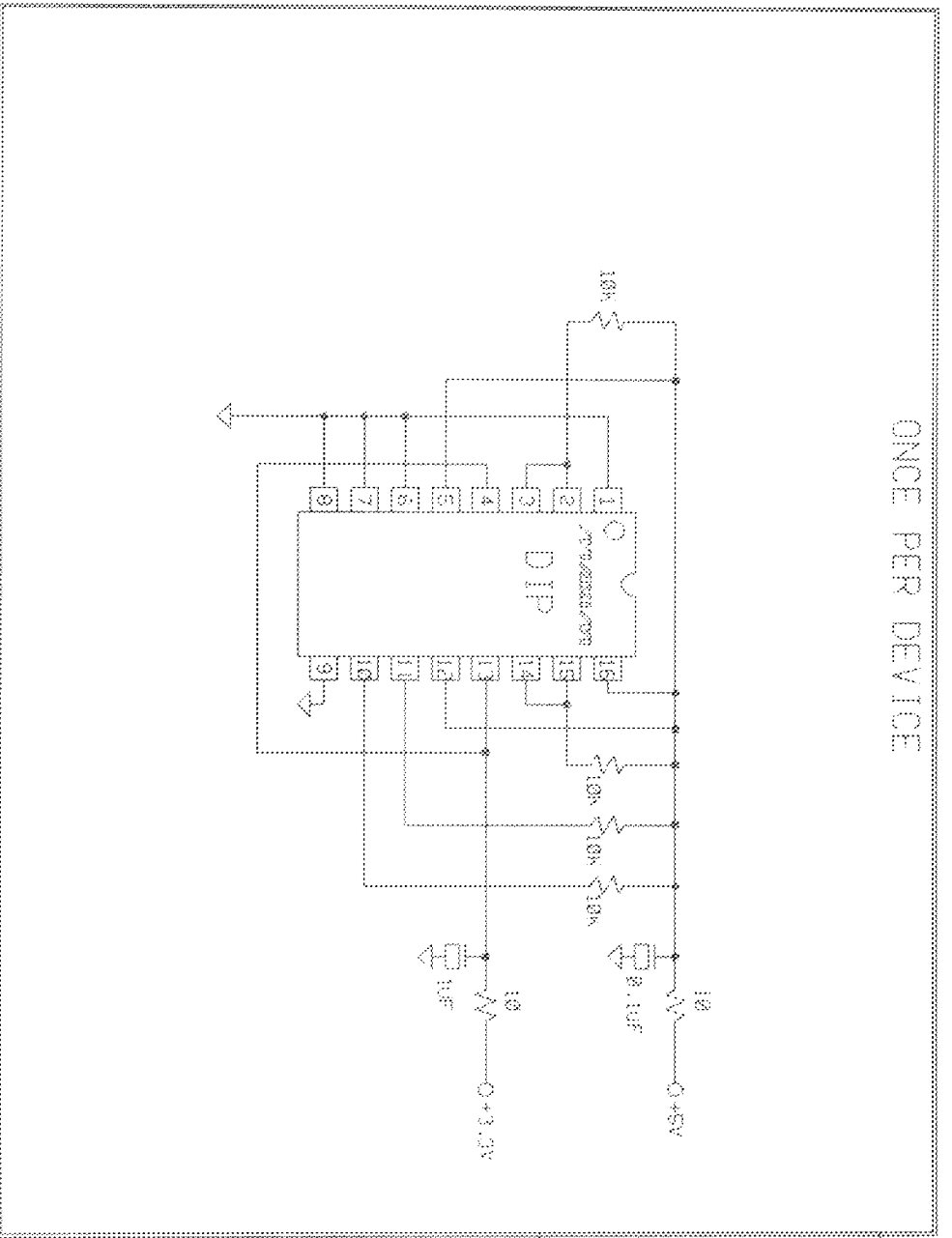
MAXIM

BUILDSHEET NUMBER:
05-0401-0493

REV.:
B

ONCE PER BOARD

ONCE PER DEVICE



--STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005
 --BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

- 1. TEMPERATURE: 125C OR EQUIVALENT
- 2. TIME: 168 HOURS MIN. OR EQUIVALENT
- 3. ALL COMPONENTS AND MATERIAL MUST STAND ISSR CONTROLS
- 4. APPROVED FOR EXJ COMMERCIAL
 EXJ RR/993

SPEC. NO. 06-5269 REV: A

DATE: 1/24/97

MAXINI BURN-IN SCHEMATIC

DEVICE TYPE: 97:

MAXISS0/SIS1

