RELIABILITY REPORT

FOR

MAX4986ETO+T

PLASTIC ENCAPSULATED DEVICES

October 21, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX4986ETO+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4986 active 2:1/1:2 multiplexer/demultiplexer equalizes and redrives SAS/SATA or SATA-only signals up to 6.0Gbps and operates from a single +3.3V supply. The MAX4986 features independent input equalization and output preemphasis. The MAX4986 enhances signal integrity at the receiver by equalizing the signal at the input and establishing preemphasis at the output of the device. SAS/SATA and SATA-only out-of-band (OOB) signaling is supported using high-speed amplitude detection on the inputs and squelch on the corresponding outputs. Inputs and outputs are internally 50 terminated and must be AC-coupled to the SAS/SATA controller IC and SAS/SATA device. The MAX4986 is available in a small (3.5mm x 9.0mm), 42-pin TQFN package optimal for simplified layout and space-saving requirements. The MAX4986C is specified over the 0°C to +70°C commercial operating temperature range. The MAX4986E is specified over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	SAS/SATA Single Lane 2:1/1:2 Multiplexer/Demultiplexer Plus Redriver with Equalization
B. Process:	G4
C. Number of Device Transistors:	5861
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan and Thailand
F. Date of Initial Production:	January 23, 2010

III. Packaging Information

A. Package Type:	42-pin TQFN 3.5x9
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3860
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	40°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	178.4 X 74.4 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1-3 = 1.2 / Metal 4 = 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1-3 = 1.6 / Metal 4 = 4.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.4 \times 10^{-9}$

λ = 23.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NZSZAQ001B, D/C 0937)

The AJ63 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX4986ETO+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0	NZSZAQ001B, D/C 0937

Note 1: Life Test Data may represent plastic DIP qualification lots.

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