RELIABILITY REPORT

FOR

MAX4970EWC+T

PLASTIC ENCAPSULATED DEVICES

February 10, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Director, Reliability Engineering

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Conclusion

The MAX4970EWC+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX4970/MAX4971/MAX4972 family of overvoltage protection devices features a low 40m (typ) RON internal FET and protect low-voltage systems against voltage faults up to +28V. These devices also drive an optional external pFET to protect against reverse-polarity input voltages. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. All switches feature a 2.3A (min) current-limit protection. During a short-circuit occurrence, the device operates in an autoretry mode where the internal MOSFET is turned on to check if the fault has been removed. The autoretry interval time is 15ms, and if the fault is removed, the MOSFET remains on. The MAX4970/MAX4971/MAX4972 feature an enable input (active-low EN) that controls the operation of the internal nFET as well as the optional external pFET. The use of active-low EN allows the external pFET to block reverse voltages independent of any signal present at the output. The overvoltage thresholds (OVLO) are preset to 4.65V (MAX4972), 5.8V (MAX4970), or 6.35V (MAX4971). The undervoltage thresholds (UVLO) are preset to 2.45V. When the input voltage drops below the UVLO, the devices enter a low-current standby mode. All devices are offered in a small 12-bump, WLP package and operate over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function: Overvoltage-Protection Controllers with a Low R_{ON} Internal FET

B. Process: S45

C. Number of Device Transistors: 1888

D. Fabrication Location: California, Texas or Japan

E. Assembly Location: Casio

F. Date of Initial Production: 4/26/2008

III. Packaging Information

A. Package Type: 12-bump WLP 3x4 Array

B. Lead Frame: na

C. Lead Finish: SAC (SnAgCu) Balls

D. Die Attach: None

E. Bondwire: na

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-9000-2995

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

A. Dimensions: 63 X 87 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 40 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 26.9 \times 10^{-9}$

λ = 26.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AJ21 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD 78.

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Table 1
Reliability Evaluation Test Results

MAX4970EWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	40	0
Moisture Testing (Note 2)				
HAST	Ta = 85°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-40°C/125°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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