

RELIABILITY REPORT
FOR
MAX4907FELA+
PLASTIC ENCAPSULATED DEVICES

June 22, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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| Approved by |
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| Quality Assurance |
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Conclusion

The MAX4907FELA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4906/MAX4906F/MAX4907/MAX4907F analog switches combine the low on-capacitance (CON) and low on-resistance (RON) necessary for high-performance switching applications. These devices are designed for USB 2.0 high-speed applications at 480Mbps. These switches will also handle all the requirements for USB low- and full-speed signaling. The MAX4906/MAX4906F feature two single-pole/double-throw (SPDT) switches, and the MAX4907/MAX4907F feature two single-pole/single-throw switches (SPST). The MAX4907/MAX4907F have a low 7 Ω (max) on-resistance and 7pF (max) on-capacitance. These devices are fully specified to operate from a single +3.0V to +3.6V power supply and are protected against a +5.5V short to COM1 and COM2. This feature makes them fully compliant with the USB 2.0 specification of +5.5V fault protection. These devices feature a low threshold voltage and a +1.4V VIH, permitting them to be used with low-voltage logic. The MAX4906/MAX4906F/MAX4907/MAX4907F operate at 300 μ A (max) quiescent current and feature a shutdown input to reduce the quiescent current to less than 2 μ A (max). The MAX4906/MAX4906F/MAX4907/MAX4907F are available in space-saving, 2mm x 2mm μ DFN packages and operate over a -40°C to +85°C temperature range.

II. Manufacturing Information

| | |
|----------------------------------|-----------------------------------|
| A. Description/Function: | High-/Full-Speed USB 2.0 Switches |
| B. Process: | S45 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | California, Texas or Japan |
| E. Assembly Location: | Thailand |
| F. Date of Initial Production: | November 23, 2005 |

III. Packaging Information

| | |
|--|--------------------------|
| A. Package Type: | 8-pin uDFN |
| B. Lead Frame: | Substrate |
| C. Lead Finish: | Gold |
| D. Die Attach: | Non-conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | n/a |
| K. Single Layer Theta Jc: | n/a |
| L. Multi Layer Theta Ja: | 210.2°C/W |
| M. Multi Layer Theta Jc: | 122.1°C/W |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 55 X 41 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

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|-----------------------------------|---|
| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 47 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 23.4 \times 10^{-9}$$

$$\lambda = 23.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AS54-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4907FELA+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|-------------|--------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 47 | 0 |
| Moisture Testing (Note 2) | | | | |
| HAST | Ta = 130°C RH = 85% Biased Time = 96hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -55°C/125°C 1000 Cycles Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data