RELIABILITY REPORT

FOR

MAX4811CTN+T

PLASTIC ENCAPSULATED DEVICES

March 24, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX4811CTN+T successfully meets the quality and reliability standards required of all Maxim Integrated products, except for ESD-HBM. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4810/MAX4811/MAX4812 integrated circuits generate high-voltage, high-frequency, unipolar or bipolar pulses from low-voltage logic inputs. These dual pulsers feature independent logic inputs, independent high-voltage pulser outputs with active clamps and independent high-voltage supply inputs. The MAX4810/MAX4811/MAX4812 feature a 9 output impedance for the high-voltage outputs, and a 27 impedance for the active clamp. The high-voltage outputs are guaranteed to provide 1.3A output current. All devices use three logic inputs per channel to control the positive and negative pulses and active clamp. Also included are two independent enable inputs. Disabling EN ensures the output MOSFETs are not accidentally turned on during fast power-supply ramping. This allows for faster ramp times and smaller delays between pulsing modes. A low-power shutdown mode reduces power consumption to less than 1µA. All digital inputs are CMOS compatible. The MAX4810 includes clamp output overvoltage protection, while the MAX4811 features both pulser output and clamp output overvoltage protection. The MAX4812 does not provide overvoltage protection. See the *Ordering Information/Selector Guide* in the full data sheet. The MAX4810/MAX4811/MAX4812 are available in a 56-pin (7mm x 7mm), TQFN exposed-pad package and are specified over the 0°C to +70°C commercial temperature range.

II. Manufacturing Information

A. Description/Function:	Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers
B. Process:	BCD250
C. Number of Device Transistors:	
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan and Thailand
F. Date of Initial Production:	July 25, 2008

III. Packaging Information

A. Package Type:	56-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3028
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	206 X 218 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1 micron (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 38 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 28.9 \times 10^{-9}$

$\lambda = 28.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the BCD250 Process results in a FIT Rate of 1.9 @ 25C and 32.7 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AJ43-1 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 500V per JEDEC JESD22-A114 (lot NKUYBQ003A, D/C 0828)
ESD-CDM:	+/- 500V per JEDEC JESD22-C101 (lot NKUYB3021B, D/C 1037)

Latch-Up testing has shown that this device withstands a current of +/- 100mA per JEDEC JESD78 (lot NKUYBQ003A, D/C 0828).

Table 1

Reliability Evaluation Test Results

MAX4811CTN+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	38	0	NKUYBQ003A, D/C 0828

Note 1: Life Test Data may represent plastic DIP qualification lots.