RELIABILITY REPORT

FOR

MAX4737EBE+T

CHIP SCALE PACKAGE

October 3, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX4737EBE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4737/MAX4738/MAX4739 low-voltage, low on-resistance (RON), quad single-pole/single throw (SPST) analog switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications. The MAX4737/MAX4738/MAX4739 feature 4.5 RON (max) with 1.2 flatness and 0.4 matching between channels. These new switches feature guaranteed operation from +1.8V to +5.5V and are fully specified at 3V and 5V. These switches offer break-before-make switching (1ns) with tON OFF <40ns at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply. These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 2mm x 2mm area and has a 4 x 4 bump array with a bump pitch of 0.5mm. These switches are also available in a 14-pin TSSOP package.

II. Manufacturing Information

A. Description/Function:	4.5 Ohm Quad SPST Analog Switches in UCSP
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas, or Oregon
E. Assembly Location:	Texas
F. Date of Initial Production:	October 24, 2002

III. Packaging Information

A. Package Type:	16-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-0210
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	135.8
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	83 X 83 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 89 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 12.3 \times 10^{-9}$

λ = 12.3 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.06 @ 25C and 0.99 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot DBH0BQ001B D/C 0420)

The AS12 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX4737EBE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	44	0	IBH0AQ001B, D/C 0234
	Biased	& functionality	45	0	DBH0BQ001B, D/C 0420
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.