RELIABILITY REPORT

FOR

MAX4688EBT-T

WAFER LEVEL PRODUCT

December 14, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX4688EBT+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4686/MAX4687/MAX4688 low on-resistance (RON), low-voltage analog switches operate from a single +1.8V to +5.5V supply. The MAX4686/MAX4687 are single-pole/single-throw (SPST) analog switches, and the MAX4688 is a single-pole/double-throw (SPDT) analog switch. The MAX4686 is a normally open (NO) switch, and the MAX4687 is a normally closed (NC) switch. The MAX4688 has one normally open (NO) switch and one normally closed (NC) switch. When powered from a 3V supply these devices feature 2.5 (max) RON, with 0.4 (max) RON matching and 1 (max) flatness. The MAX4686/MAX4687/MAX4688 offer fast switching speeds (tON = 30ns max, tOFF = 12ns max). The MAX4688 offers break-before-make action. The digital logic inputs are 1.8V logic compatible from a +2.7V to +3.3V supply. The MAX4686/MAX4687/MAX4688 are available in the chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 1.50mm x 1.02mm area. The 3 x 2 array of solder bumps are spaced with a 0.5mm bump pitch.

II. Manufacturing Information

A. Description/Function:	2.5 , Low-Voltage, SPST/SPDT Analog Switches in UCSP Package
B. Process:	TS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Arizona
F. Date of Initial Production:	April 28, 2001

III. Packaging Information

A. Package Type:	6-pin uCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-1201-0209
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	259.5°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	59 X 40 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50µm F.
Minimum Metal Spacing:	0.50µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot K31CAQ002C D/C 0030)

The AH72-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-200V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4688EBT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	K31CAQ002C, D/C 0030

Note 1: Life Test Data may represent plastic DIP qualification lots