

RELIABILITY REPORT

FOR

MAX4641EUA+T

PLASTIC ENCAPSULATED DEVICES

September 27, 2017

MAXIM INTEGRATED

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Conclusion

The MAX4641EUA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4641/MAX4642/MAX4643 are monolithic, dual, single-pole/single-throw (SPST) switches that can operate from a single supply ranging from +1.8V to +5.5V. The MAX4641/MAX4642/MAX4643 provide low 4 on-resistance (RON), 0.6 RON matching between channels, and 1 RON flatness over the entire analog signal range. These devices offer fast switching times of less than 20ns while consuming less than 0.01µW of quiescent power. The MAX4641 has two normally open (NO) switches, and the MAX4642 has two normally closed (NC) switches. The MAX4643 has one NO switch and one NC switch. All three devices have low 0.35nA leakage currents over the entire temperature range. The MAX4641/MAX4642/MAX4643 are available in small 8-pin µMAX® and 8-pin QFN packages.



II. Manufacturing Information

A. Description/Function: High-Speed, Low-Voltage, 4 Ohm, Dual SPST CMOS Analog Switches

B. Process: TS50C. Fabrication Location: Taiwan

D. Assembly Location: Philippines, Thailand

E. Date of Initial Production: April 22, 2000

III. Packaging Information

A. Package Type: 8-pin uMAX
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)

F. Mold Material: Epoxy with silica filler
 G. Assembly Diagram: #05-1201-0160
 H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity Level 1

per JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 221°C/W
K. Single Layer Theta Jc: 41.9°C/W
L. Multi Layer Theta Ja: 206.3°C/W
M. Multi Layer Theta Jc: 41.9°C/W

IV. Die Information

A. Dimensions: 50X35 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.50 microns (as drawn)F. Minimum Metal Spacing: 0.50 microns (as drawn)

G. Isolation Dielectric: SiO₂H. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)

Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (೩) is calculated as follows:

$$\frac{\lambda = 1}{\text{MTTF}} = \frac{1.83 \quad \text{(Chi square value for MTTF upper limit)}}{192 \times 4340 \times 240 \times 2}$$

$$\text{(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)}$$

$$\lambda = 4.6 \times 10^{-9}$$

$$\lambda = 4.6 \text{ F.I.T. (60% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AH42 die type has been found to have all pins able to withstand an HBM transient pulse of +/-400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX4641EUA+T

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|------------------------|---------------------------------------|----------------------------------|-------------|-----------------------|
| Static Life Test (Note | e 1) Ta = 135C Biased Time = 192 hrs. | DC Parameters & functionality | 240 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.