RELIABILITY REPORT

FOR

MAX4638Exx

PLASTIC ENCAPSULATED DEVICES

June 20, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4638 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4638 is a single 8:1 CMOS analog multiplexers/demultiplexers (muxes/ demuxes). The mux operates from a single +1.8V to +5V supply or dual ±2.5V supplies. This device features 3.5Ω on-resistance (R_{ON}) when powered with a single +5V supply and has -75dB of off-isolation and -85dB crosstalk from the output to each off channel. The switching times are 18ns t_{ON} and 7ns t_{OFF}. It features a -3dB 85MHz bandwidth and a guaranteed 0.25nA leakage current at +25°C.

A +1.8V to +5.5V operating range makes the MAX4638 ideal for battery-powered, portable instruments. All channels guarantee break-before-make switching. This part features bidirectional operation and can handle Rail-to-Rail® analog signals. All control inputs are TTL/CMOS-logic compatible. Decoding is in standard BCD format, and an enable input is provided to simplify cascading of devices. This devices are available in small 16-pin QFN, TSSOP and SOIC packages, as well as a 20-pin QFN package.

B. Absolute Maximum Ratings

Item	Rating
(Voltages Referenced to GND)	
V+ to V-	+6V
V+, A_, EN	-0.3V to +6V
V-	+0.3V to -6V
NO_, COM_ (Note1)	-0.3V to (V+ + 0.3V)
Continuous Current A_, EN	±30mA
Continuous Current NO_, COM_	±100mA
Peak Current (NO_, COM_) (pulsed at 1ms, 10% duty cycle)	±200mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature.	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QFN (4x4)	1481mW
16-Pin TSSOP	457mW
16-Pin SO	696mW
20-Pin QFN (4x4)	1600mw
Derates above +70°C	
16-Pin QFN (4x4	18.5mW/°C
16-Pin TSSOP	5.7mW/°C
16-Pin SO	8.7mW/°C
20-Pin QFN (4x4))	20.0mW/°C

Note 1: Signals on COM_, NO_ exceeding V+ or V- are clamped by internal diodes. A_ and EN are clamped only to V- and can exceed V+ up to their maximum ratings. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	3.5Ω, Single 8:1, Low-Voltage Analog Multiplexers
B. Process:	TC05 (0.5 micron CMOS)
C. Number of Device Transistors:	632
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Malaysia, Thailand, Korea or Philippines
F. Date of Initial Production:	July, 2000

III. Packaging Information

A. Package Type:	**16-Pin QFN(4x4)**	**16-Pin TSSOP**	**16-Pin SO**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0282	# 05-1201-0193	# 05-1201-0194
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

III. Packaging Information

A. Package Type:	**20-Pin QFN (4x4)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0284
I. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	66 x 70 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.5 microns; Metal 2: 0.7 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.5 microns; Metal 2: 0.7 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ λ= 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5642) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH70 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX4638Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN TSSOP SO	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

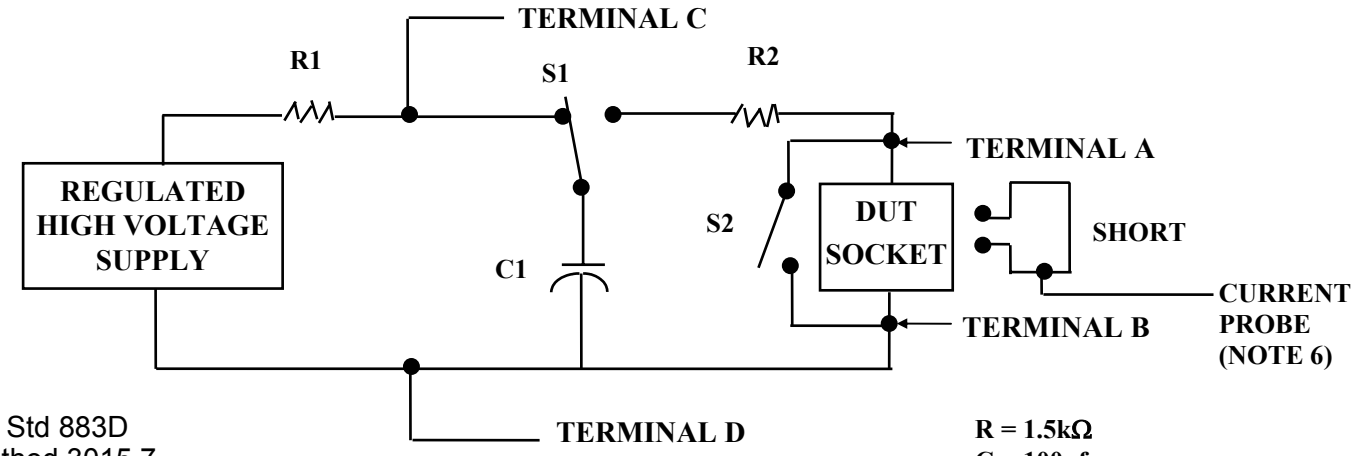
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

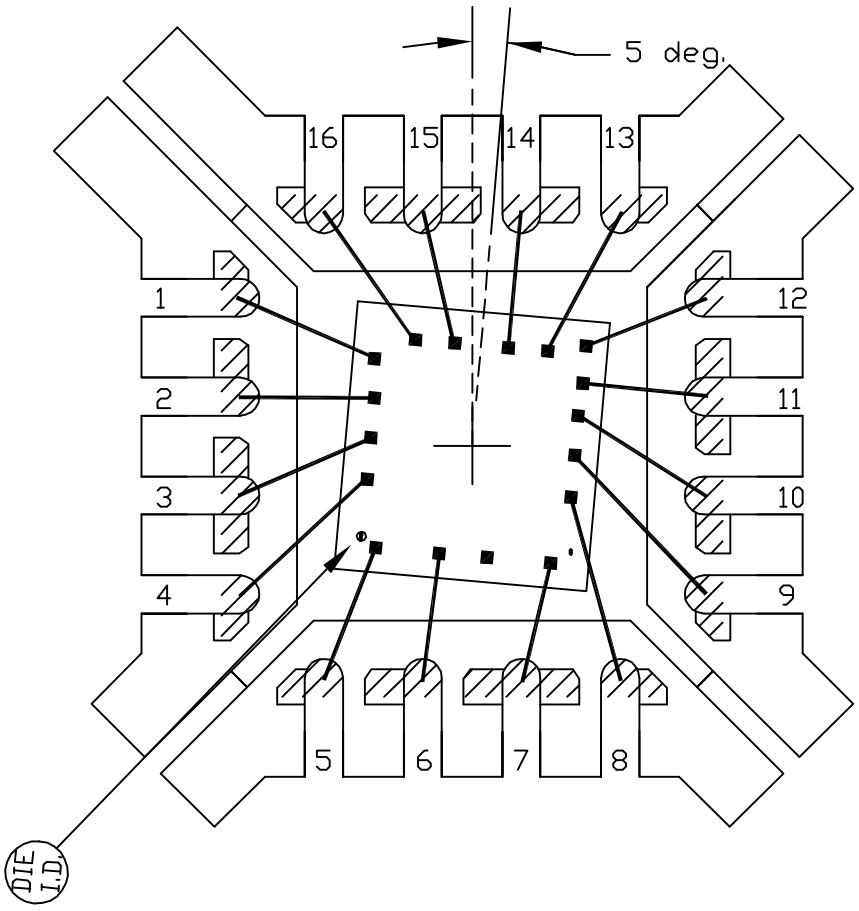
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



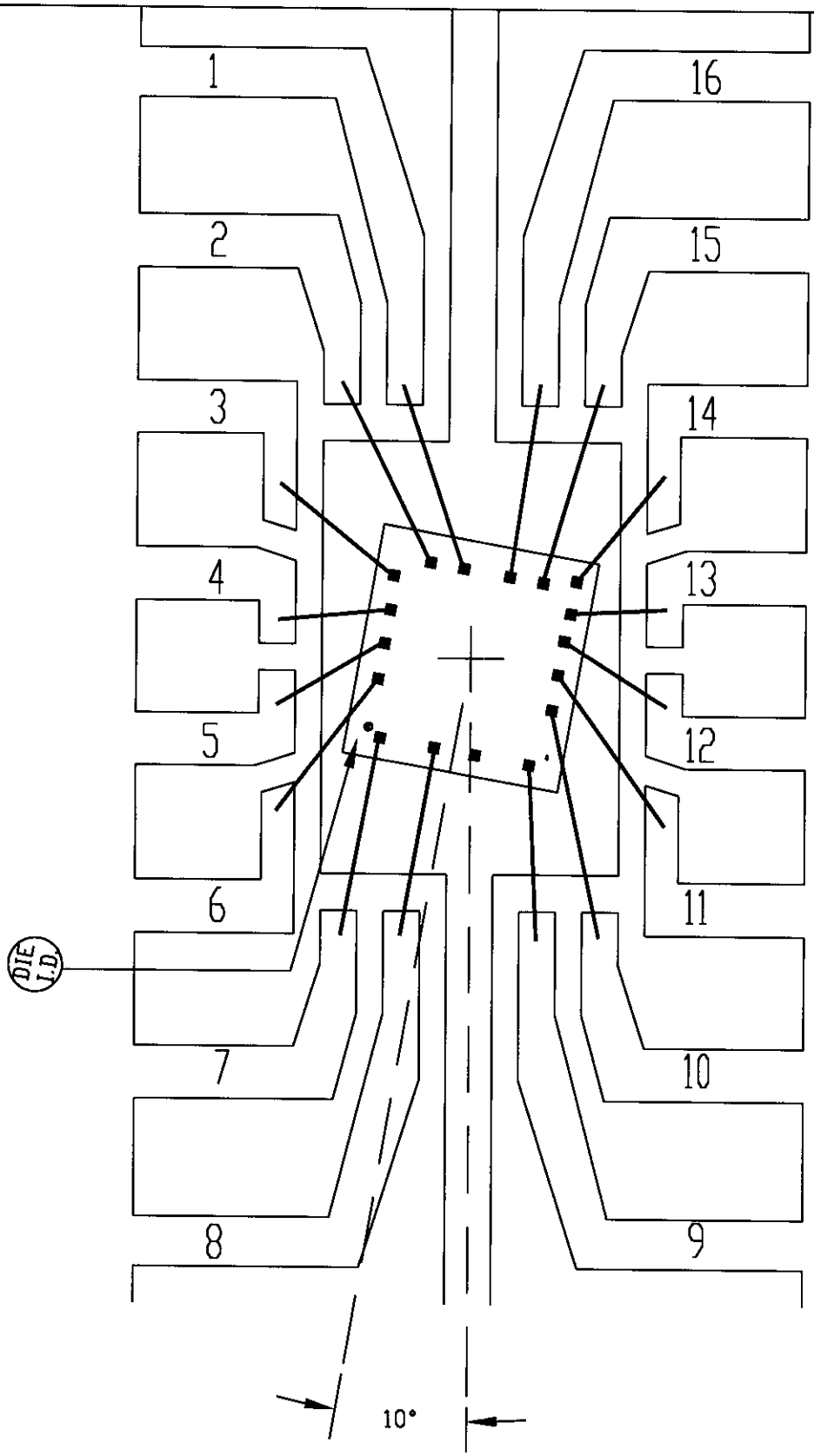
EXPOSED PAD PKG.



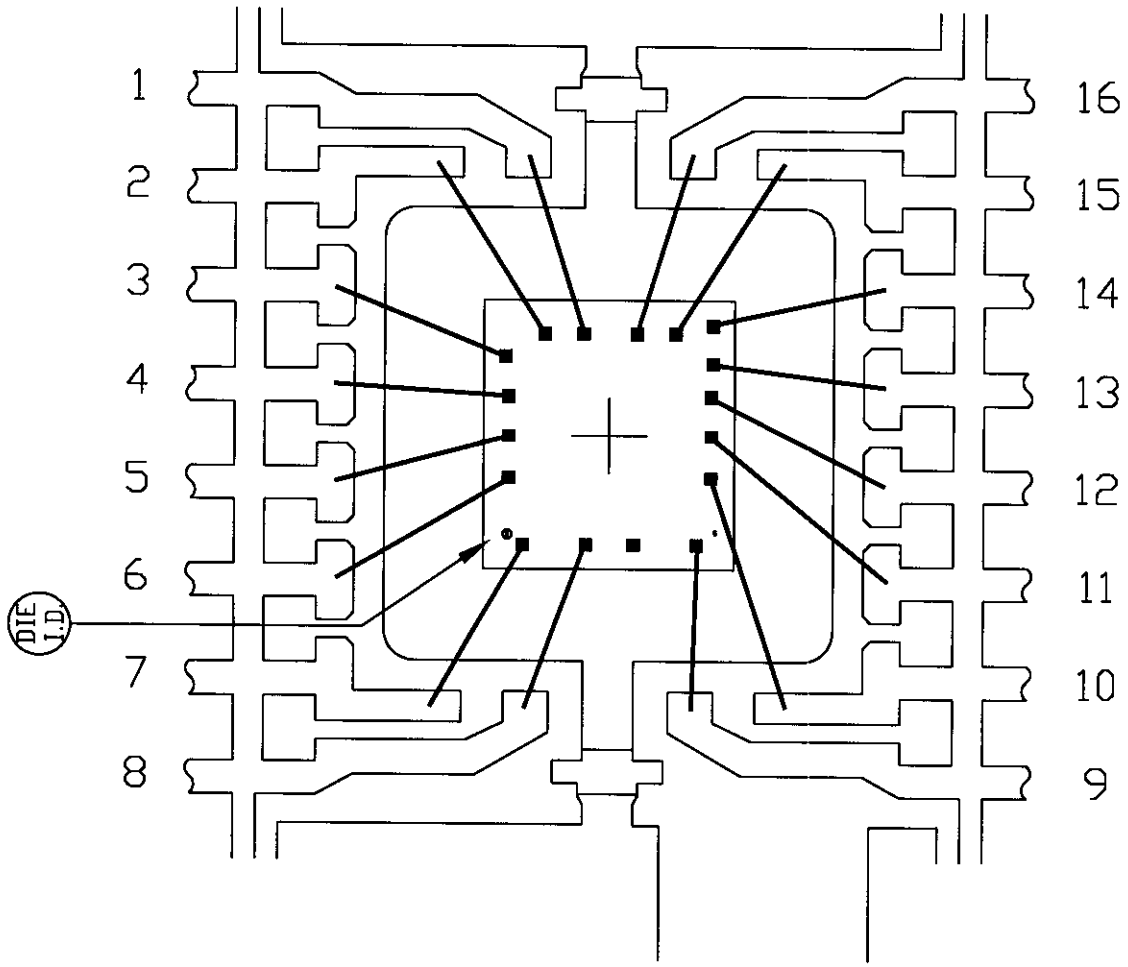
BONDABLE AREA

PKG. BODY SIZE: 4x4 mm

PKG. CODE: G1644-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 91x91	PKG.			BOND DIAGRAM #: 05-1201-0282	REV: A
	DESIGN				

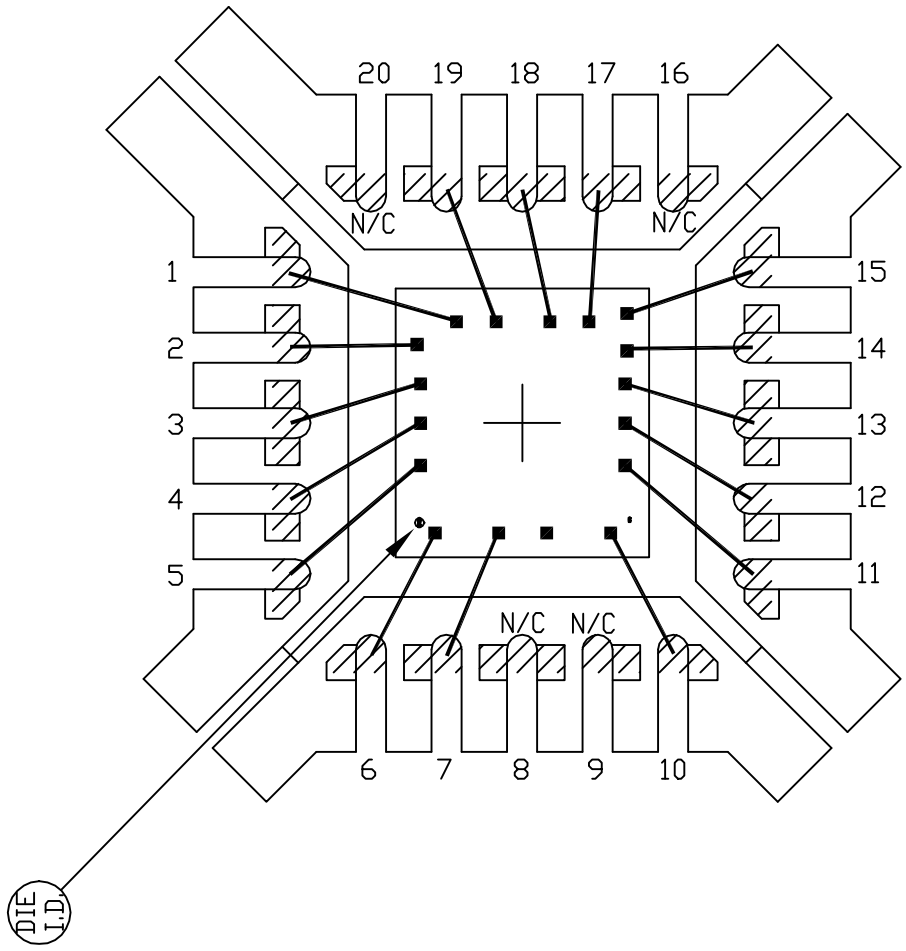


PKG. CODE: S16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0194 REV: A



PKG. CODE: U16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 118X118	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0193 / REV: A

EXPOSED PAD PKG.



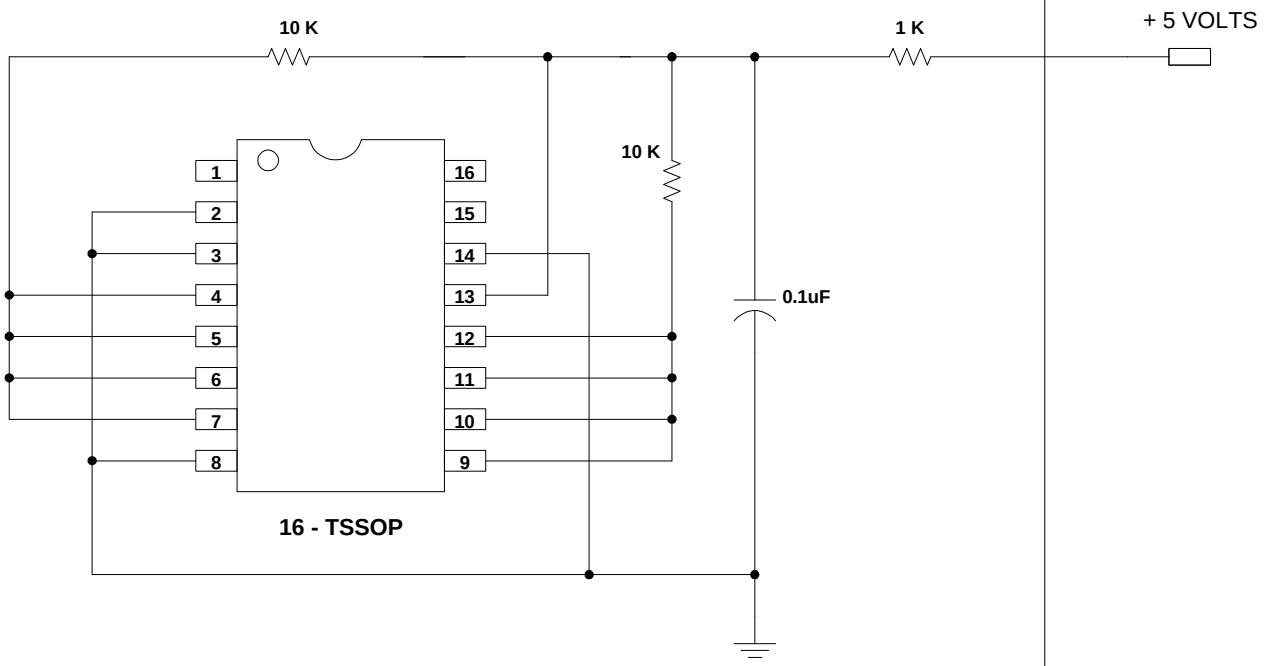
BONDABLE AREA

PKG. BODY SIZE: 4x4 mm

PKG. CODE: G2044-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 91x91	PKG.			BOND DIAGRAM #: 05-1201-0284	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4638

MAX. EXPECTED CURRENT = 10uA

DRAWN BY: HAK TAN

NOTES: