RELIABILITY REPORT

FOR

MAX4633ESE+T

PLASTIC ENCAPSULATED DEVICES

August 18, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX4633ESE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4631/MAX4632/MAX4633 high-voltage, dual analog switches are pin compatible with the industry-standard DG401/DG403/DG405. They upgrade the existing devices with fault-protected inputs and rail-to-rail signal handling capabilities. The MAX4631/MAX4632/MAX4633's normally open (NO) and normally closed (NC) terminals are protected from overvoltage faults up to 36V during power-up or power-down. During a fault condition, these terminals become open circuit and only nano-amperes of leakage current flow from the source, yet the switch output (COM_) continues to furnish up to 18mA of the appropriate polarity supply voltage to the load. This ensures unambiguous rail-to-rail outputs when a fault begins and ends. On-resistance is 85 (max) at +25°C and is matched between switches to 6 (max). Off-leakage current is only 0.5nA at +25°C and 5nA at +85°C. The MAX4631 has two NO single-pole/single-throw (SPST) switches. The MAX4632 has two NO/NC single-pole/double-throw (SPDT) switches. The MAX4633 has two NO double-pole/single-throw (DPST) switches. These CMOS switches operate with dual power supplies ranging from ±4.5V to ±18V or a single supply between +9V and +36V. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±15V or a single +12V supply.

II. Manufacturing Information

A. Description/Function:	Fault-Protected, High-Voltage, Dual Analog Switches
B. Process:	S5
C. Number of Device Transistors:	2064
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	July 24, 1999

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	85Sn/15Pb plate
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1201-0098
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	115°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	71°C/W
M. Multi Layer Theta Jc:	23°C/W

IV. Die Information

A. Dimensions:	86 X 128 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.9 \times 10^{-9}$

$\lambda = 6.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25°C and 1.55 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AH21-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-400V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX4633ESE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.