RELIABILITY REPORT

FOR

MAX4533xxP

PLASTIC ENCAPSULATED DEVICES

July 21, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4533 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4533 quad, single-pole/double-throw (SPDT), fault-protected analog switch is pin-compatible with the industry-standard MAX333 and MAX333A. The MAX4533 features fault-protected inputs and Rail-to-Rail® signal handling. The normally open (NO_) and normally closed (NC_) terminals are protected from overvoltage faults up to ±25V with power on and up to ±40V with power off. During a fault condition, NO_ and NC_ become high impedance with only nanoamperes of leakage current flowing to the source. In addition, the output (COM_) clamps to the appropriate polarity supply rail and provides up to ±10mA of load current. This ensures unambiguous rail-to-rail outputs when a fault occurs.

The MAX4533 operates from dual ±4.5V to ±18V power supplies or a single +9V to +36V supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility when using ±15V supplies or a +12V supply. On-resistance is 175Ω max and is matched between switches to 10Ω max. The off-leakage current is only 0.5nA at T_A = +25°C and 10nA at T_A = +85°C.

B. Absolute Maximum Ratings

Item	Rating
Voltages Referenced to GND	
V+	-0.3V to +44.0V
V-	-44.0V to +0.3V
V+ to V-	-0.3V to +44.0V
COM_, IN_ (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
NC_, NO_ (Note 2)	(V+ - 40V) to (V- + 40V)
NC_, NO_ to COM_	-40V to +40V
NC_, NO_ Overvoltage with Switch Power On (supplies at ±15V)	-30V to +30V
NC_, NO_ Overvoltage with Switch Power Off	-40V to +40V
Continuous Current into Any Terminal	±30mA
Peak Current into Any Terminal(pulsed at 1ms,10% duty cycle)	±50mA
Operating Temperature Ranges	
MAX4533C_ _	0°C to +70°C
MAX4533E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin Plastic DIP	889mW
20-Pin Wide SO	800mW
20-Pin SSOP	842mW
Derates above +70°C	
20-Pin Plastic DIP	11.11mW/°C
20-Pin Wide SO	10.00mW/°C
20-Pin SSOP	10.53mW/°C

Note 1: COM_ and IN_ pins are not fault protected. Signals on COM_ or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: NC_ and NO_ pins are fault protected. Signals on NC_ or NO_ exceeding -25V to +25V may damage the device. These limits apply with power applied to V+ or V-. The limit is ±40V with V+ = V- = 0.

II. Manufacturing Information

A. Description/Function:	Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch
B. Process:	S5HV - Medium voltage 5 micron silicon gate CMOS
C. Number of Device Transistors:	448
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Thailand or Malaysia
F. Date of Initial Production:	March, 1999

III. Packaging Information

A. Package Type:	**20-Lead WSO**	**20-Lead PDIP**	**20-Lead SSOP**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0861	#05-0301-0859	#05-0301-0860
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	114 x 166 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-3190) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG99-2 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4533xxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP WSO SSOP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

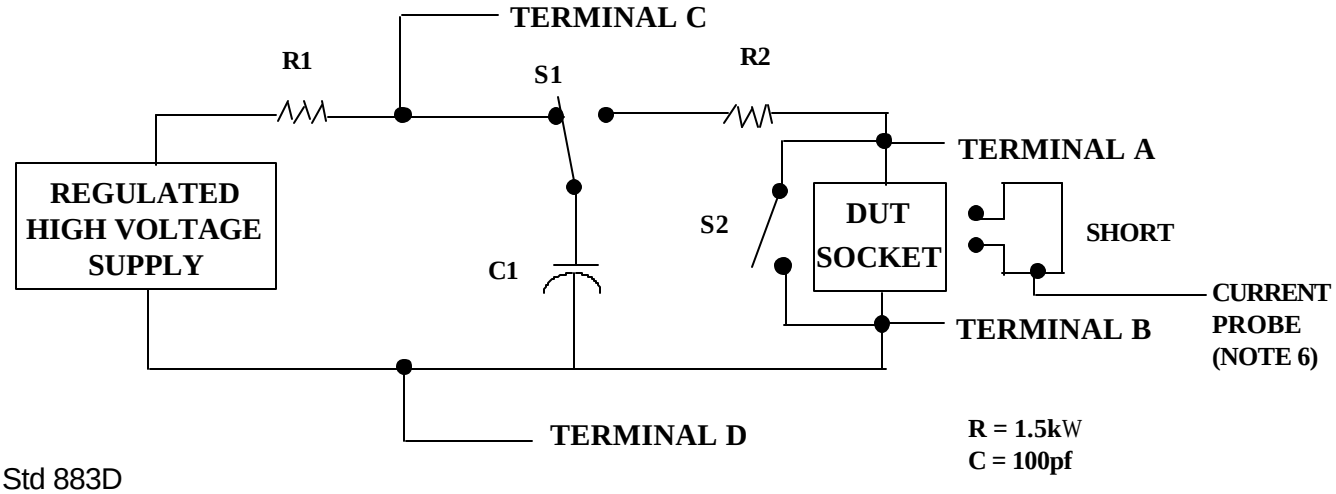
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

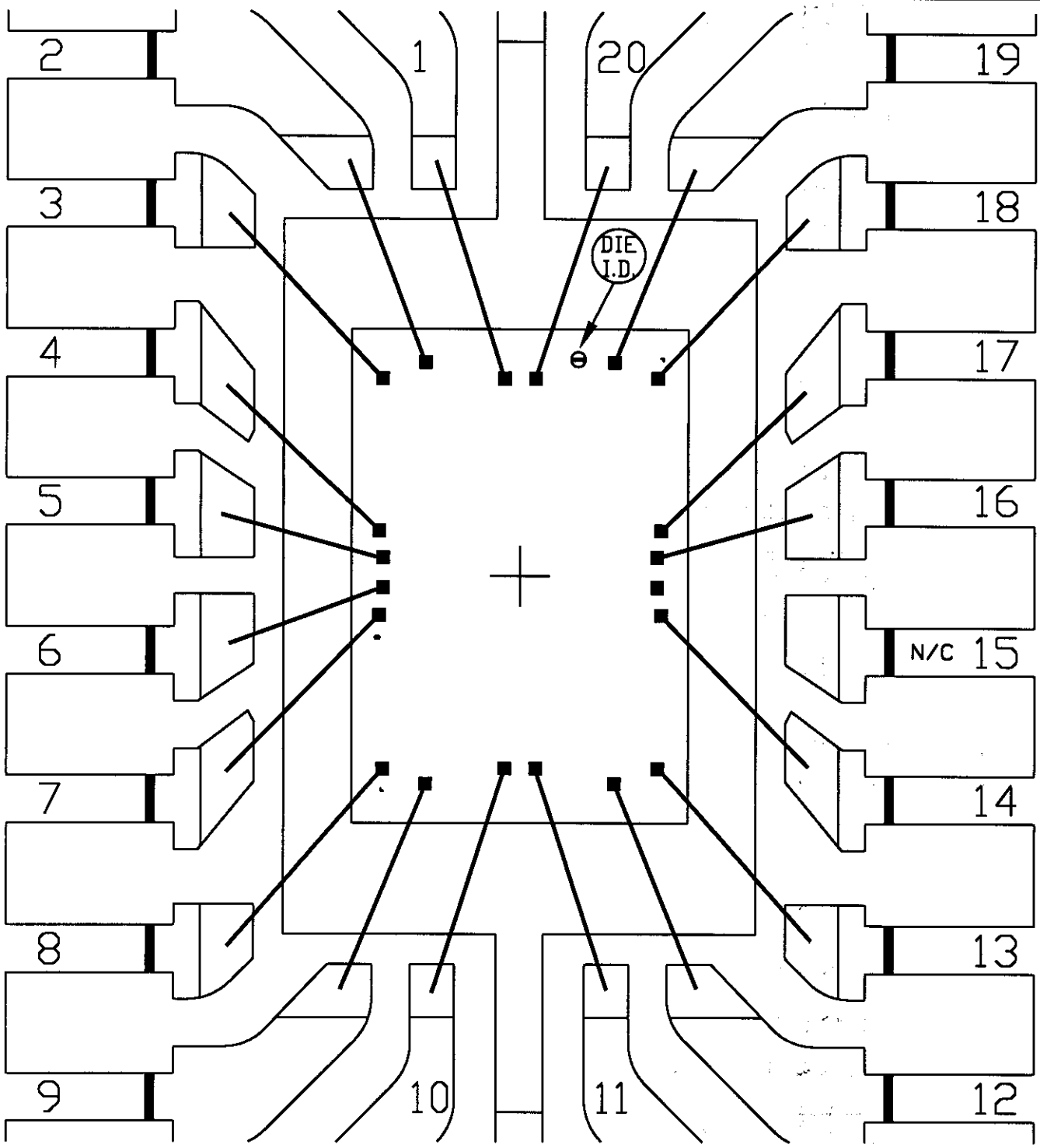
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

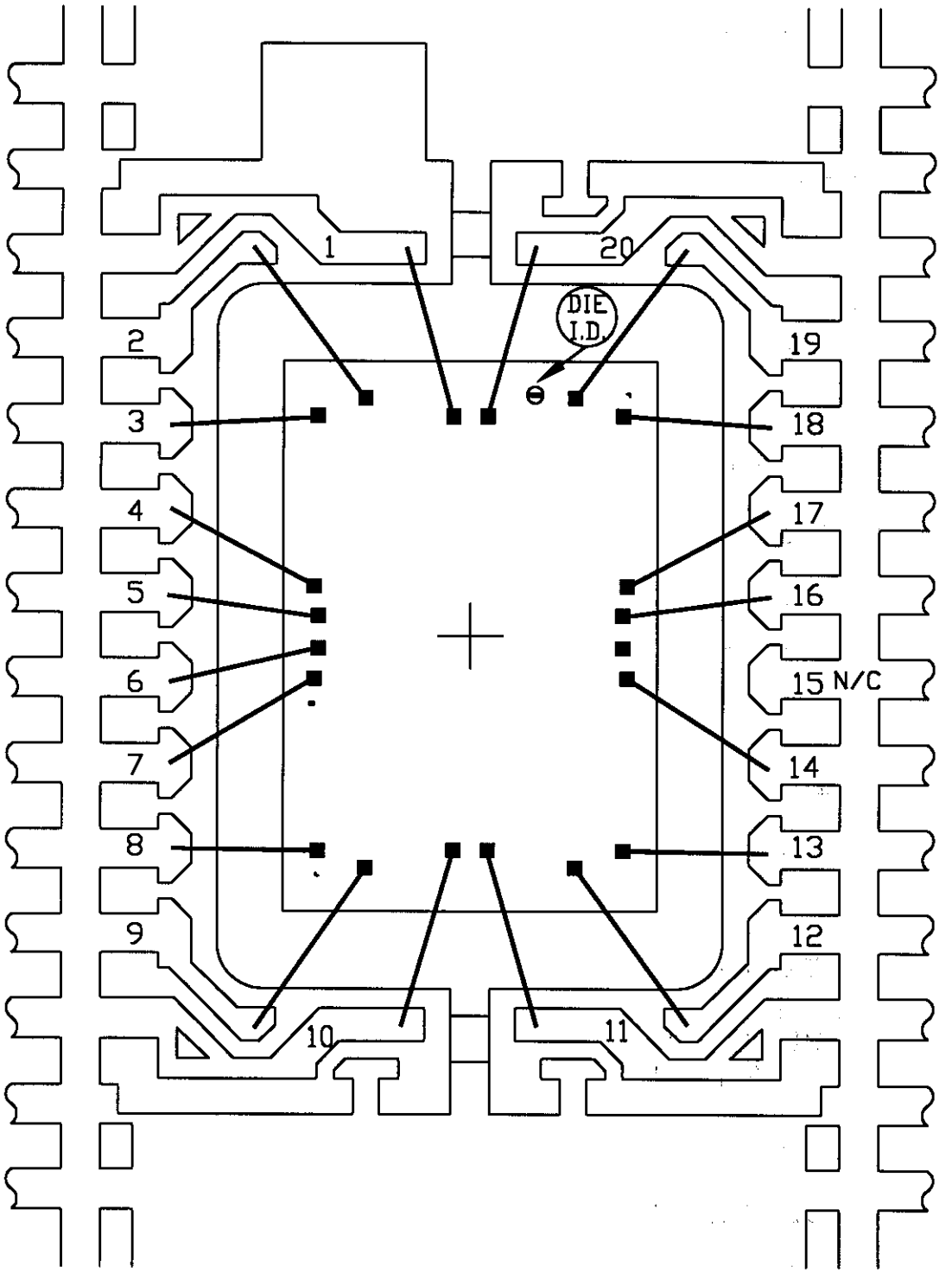
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



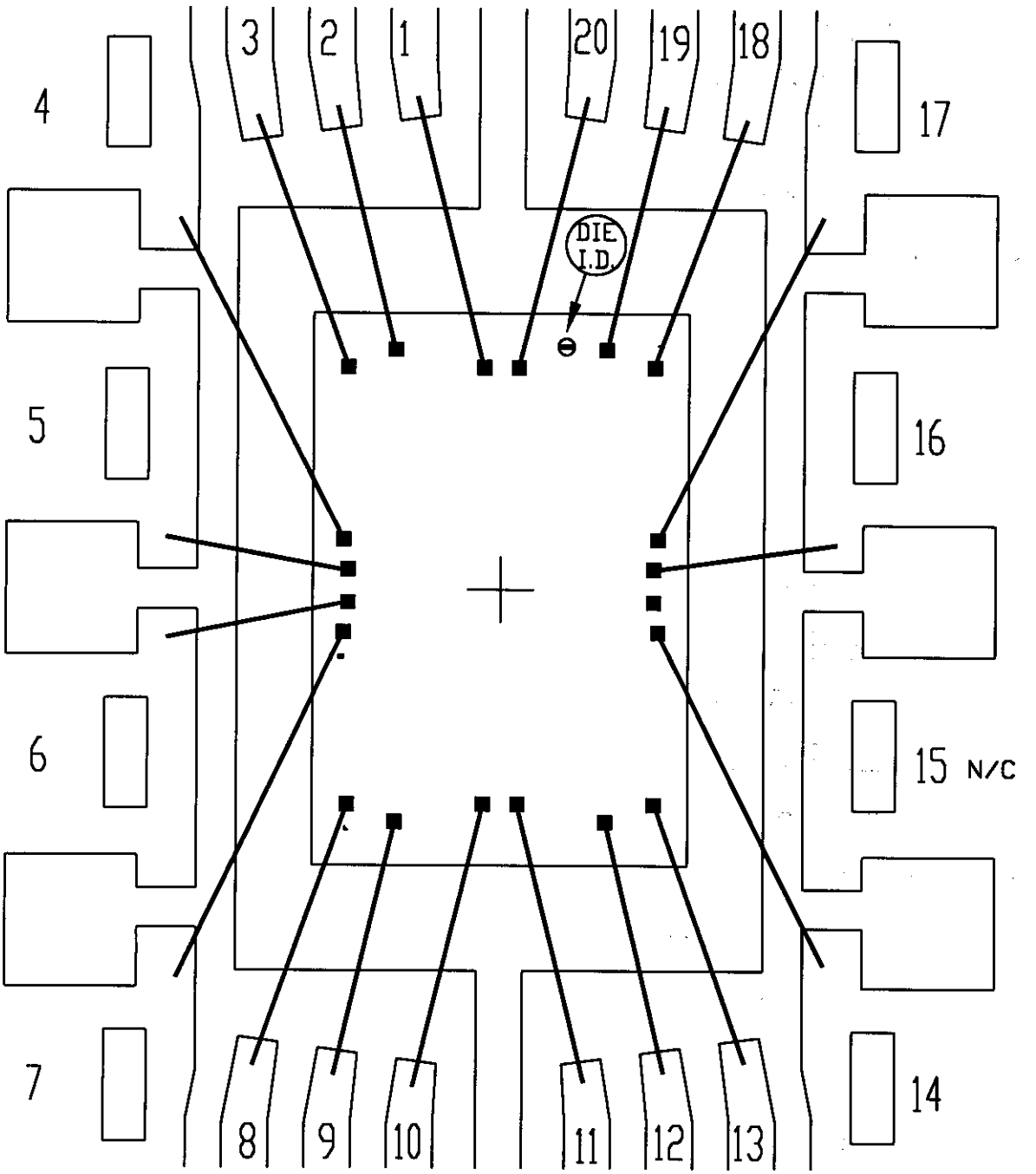
Mil Std 883D
Method 3015.7
Notice 8



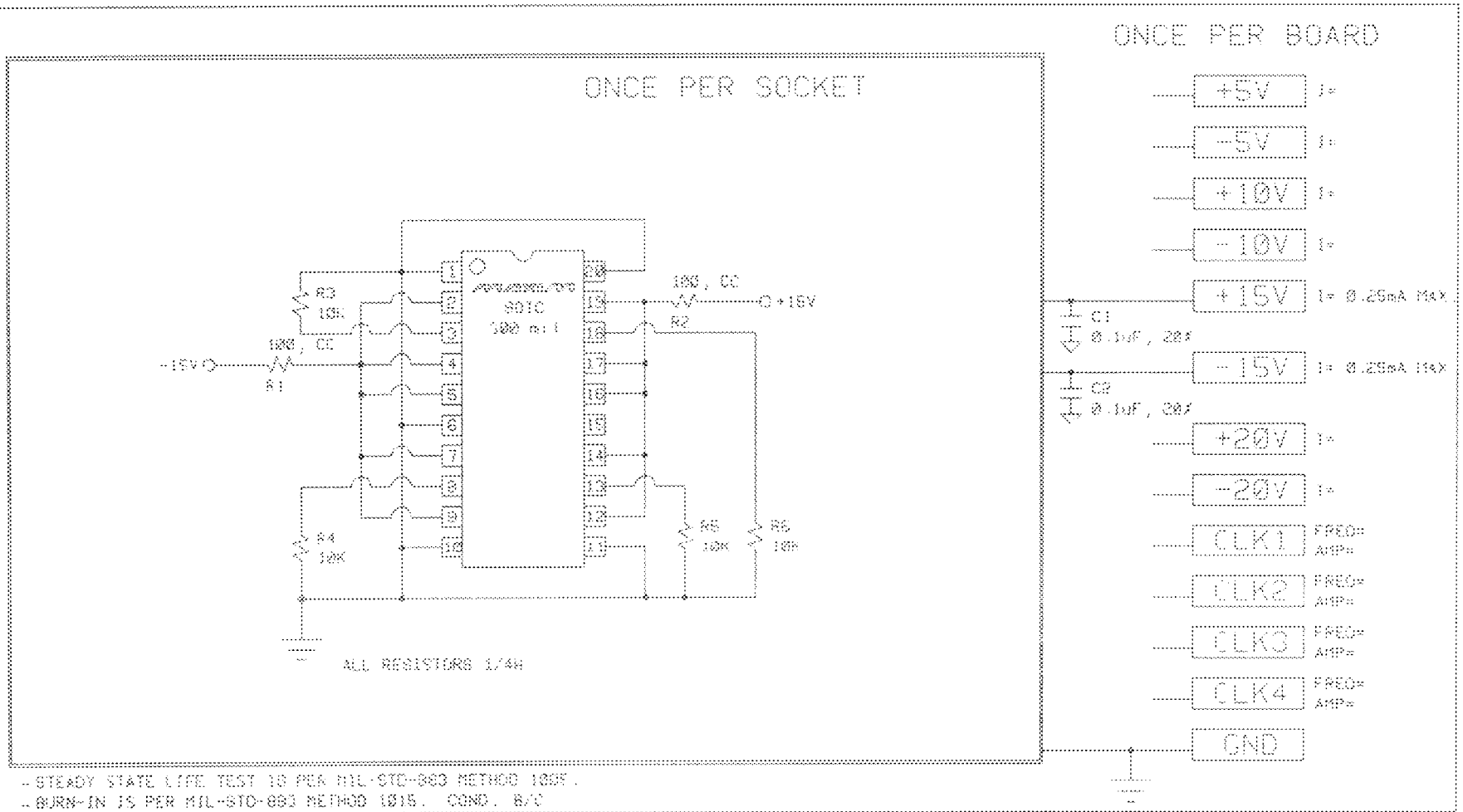
PKG.CODE: W20-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 160X240	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0861 / REV.: A



PKG.CODE: A20-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 154X213	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0860 / REV.: A



PKG.CODE: P20-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 160 X 230	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0859 / REV.: A



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B/C

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-3190 REV. A

DATE: 7/14/92

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX333