

RELIABILITY REPORT
FOR
MAX44242AKA+T
PLASTIC ENCAPSULATED DEVICES

April 3, 2014

MAXIM INTEGRATED

160 RIO ROBLES SAN JOSE, CA 95134

| Approved by | | | | | |
|-------------------------|--|--|--|--|--|
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| Quality Assurance | | | | | |
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Conclusion

The MAX4424AKA+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description

IV.Die Information

II.Manufacturing Information

V.Quality Assurance Information

III.Packaging Information

VI.Reliability Evaluation

.....Attachments

I. Device Description

A. General

The MAX44242 provides a combination of high voltage, low noise, low input bias current in a dual channel and features rail-to-rail at the output. This dual amplifier operates over a wide supply voltage range from a single 2.7V to 20V supply or split ± 1.35 V to ± 10 V supplies and consumes only 1.2mA quiescent supply current per channel. The MAX44242 is a unity-gain stable amplifier with a gain-bandwidth product of 10MHz. The device outputs drive up to 200pF load capacitor without any external isolation resistor compensation. The MAX44242 is available in 8-pin SOT23 and μ MAX packages and is rated for operation over the -40°C to +125°C automotive temperature range.



II. Manufacturing Information

A. Description/Function: 20V, Low Input Bias-Current, Low-Noise, Dual Op Amplifier

B. Process: S18C. Number of Device Transistors: 539D. Fabrication Location: USA

E. Assembly Location: Malaysia, ThailandF. Date of Initial Production: December 17, 2013

III. Packaging Information

A. Package Type: 8-pin SOT23 8-pin μ Max B. Lead Frame: Copper Copper

C. Lead Finish: 100% matte Tin 100% matte Tin D. Die Attach: Conductive Conductive E. Bondwire: Au (0.8 mil dia.) Au (0.8 mil dia.) F. Mold Material: Epoxy with silica filler Epoxy with silica filler G. Assembly Diagram: #05-9000-5339 #05-9000-5340 H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity Level 1 Level 1

per JEDEC standard J-STD-020-C

J. Single Layer Theta Jb: 110°C/W
K. Single Layer Theta Jc: 80°C/W
L. Multi Layer Theta Ja: 196°C/W
M. Multi Layer Theta Jc: 70°C/W
42°C/W

IV. Die Information

A. Dimensions: 76.7716 X 23.622 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn)F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm
D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (3) is calculated as follows:

$$\lambda = 1 \over \text{MTTF}$$
 = 1.83 (Chi square value for MTTF upper limit)
 $192 \times 4340 \times 80 \times 2$ (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

 $\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OZ01-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX44242AKA+T

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---------------------|-----------------|---------------------------|-------------|-----------------------|----------|
| Static Life Test (N | Note 1) | | | | |
| | Ta = 135°C | DC Parameters | 80 | 0 | |
| | Biased | & functionality | | | |
| | Time = 192 hrs. | | | | |

Note 1: Life Test Data may represent plastic DIP qualification lots.