RELIABILITY REPORT

FOR

**MAX4400AxK**

PLASTIC ENCAPSULATED DEVICES

May 18, 2003

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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**Conclusion**

The MAX4400 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



## I. Device Description

### A. General

The MAX4400 low cost, general-purpose op amp offers Rail-to-Rail® outputs, draws only 320µA of quiescent current, and operates from a single +2.5V to +5.5V supply. This device delivers ±1.4mA of output current and is unity-gain stable with a 1MHz gain-bandwidth product driving capacitive loads up to 400pF. The MAX4400 is specified to +125°C, making it suitable for use in a variety of harsh environments, such as automotive applications.

The MAX4400 single amplifier is available in ultra-small 5-pin SC70 and space-saving 5-pin SOT23 packages.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Power-Supply Voltage (VDD to VSS) | -0.3V to +6V |
| All Other Pins | (VSS - 0.3V) to (VDD + 0.3V) |
| Output Short-Circuit DurationOUT Shorted to VSS or VDD | Continuous |
| Operating Temperature Range | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 5-Pin SOT23 | 571mW |
| 5-Pin SC70 | 200mW |
| Derates above +70°C | |
| 5-Pin SOT23 | 7.1mW/°C |
| 5-Pin SC70 | 2.5mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Single, Low-Cost, Single-Supply,Rail-to-Rail Op Amps with Shutdown |
| B. Process: | S8 (Standard 0.8 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 101 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Malaysia, Philippines or Thailand |
| F. Date of Initial Production: | January, 2000 |

## III. Packaging Information

| | | |
|---|---|---|
| A. Package Type: | **5-Pin SOT23** | **5-Pin SC70** |
| B. Lead Frame: | Copper | Copper or Alloy 42 |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1 mil dia.) | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-2501-0018 | # 05-2501-0019 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 30 x 31 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.8 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.8 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5662) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OX05 die type has been found to have all pins able to withstand a transient pulse of ±2000V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

**Table 1**
Reliability Evaluation Test Results

**MAX4400AxK**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | SOT23<br>SC70 | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

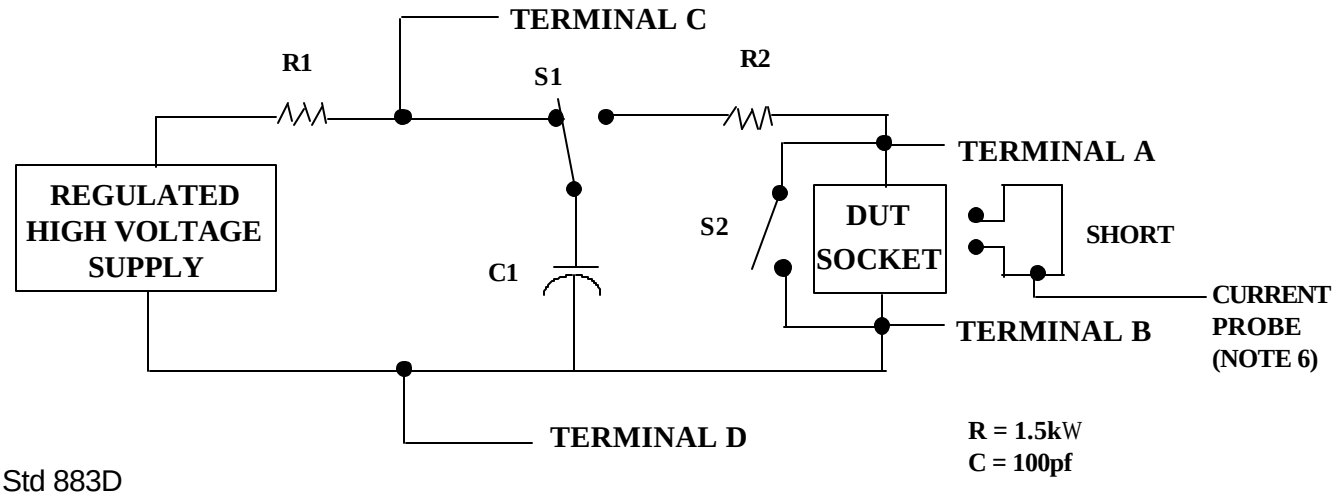
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

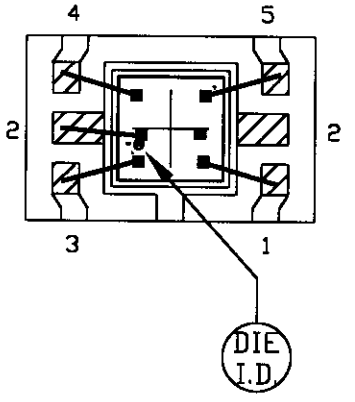
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



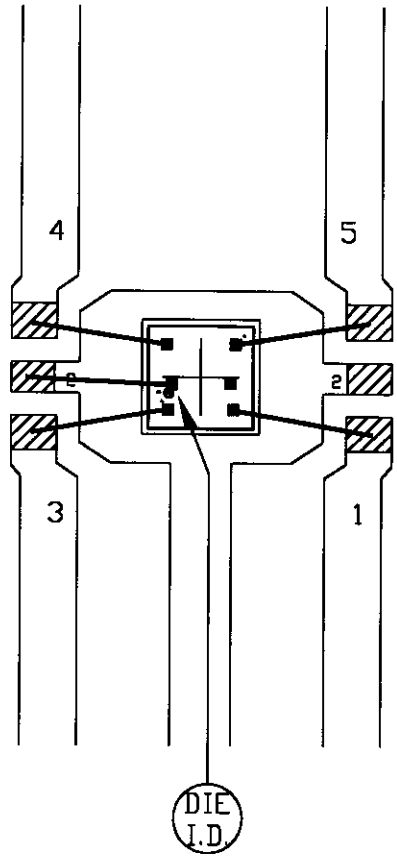

Mil Std 883D
Method 3015.7
Notice 8




▨ BONDABLE AREA

NOTE: CAVITY DOWN

| | | | | |
|---|---|---|---|---|
| PKG.CODE: X5-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 35x34 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-2501-0019 / REV.: A |



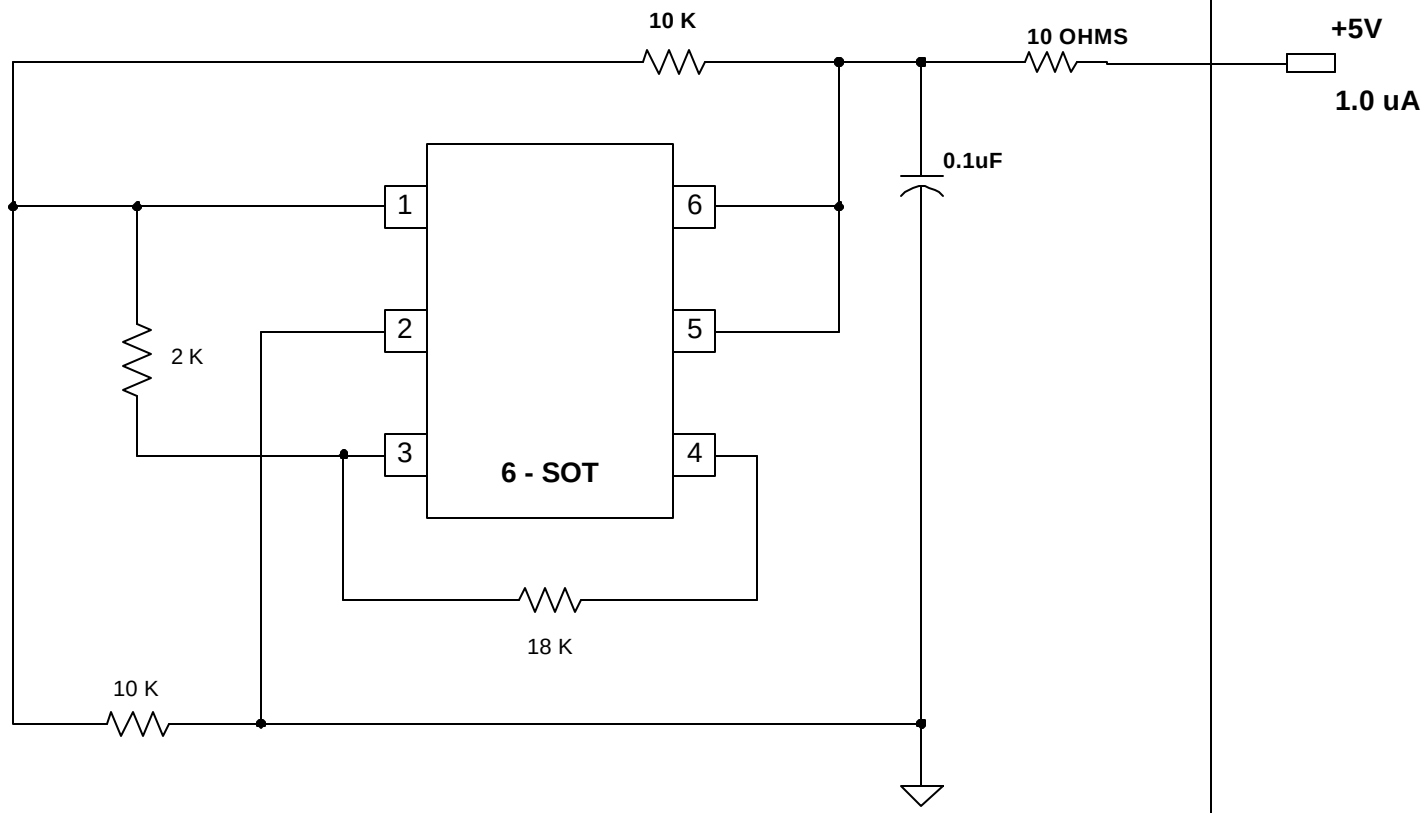

▨ - BONDING AREA

NOTE: CAVITY DOWN

| | | | | |
|---|---|---|---|---|
| PKG.CODE: U5-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 64X45 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-2501-0018 / REV.: A |

ONCE PER SOCKET

**ONCE PER BOARD**




DEVICES: MAX 4464/4470/4400/4401/4480/4481/
4490/4291/4465/4466/4335/4336/4245/LMX321/4231
MAX CURRENT: MAX4481/MAX4291/LMX321= 800uA / MAX4464/4470/
4480/4465/4466= 400uA / MAX4400/4401/4245=1.2mA / MAX4490=2.5mA
MAX4435/4436/4231/4230=3.4mA