RELIABILITY REPORT FOR

MAX40200ANS+T / MAX40200AUK+T

WAFER LEVEL DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX40200ANS+T / MAX40200AUK+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX40200 is an ideal diode current-switch that drops so little voltage that it approaches an order of magnitude better than Schottky diodes. When forward-biased and enabled, the MAX40200 conducts with as little as 85mV of voltage drop while carrying currents as high as 1A. Typical voltage drop is 43mV at 500mA, with the voltage drop increasing linearly at higher currents. The MAX40200 thermally protects itself, and any downstream circuitry, from overtemperature conditions.

When disabled (EN = low) the MAX40200 blocks voltages up to 6V in either direction, making it suitable for most low-voltage, portable electronic devices. The MAX40200 operates from a supply voltage of 1.5V to 5.5V. The MAX40200 is available in a tiny, 0.73mm X 0.73mm, 4-bump wafer-level package (WLP), with a 0.35mm bump pitch and only 0.5mm high and 5-pin SOT-23 package. The MAX40200 operates over the extended -40°C to +125°C temperature range.

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II. Manufacturing Information

A. Description/Function:	Ultra-Tiny Micropower, 1A Ideal Diode with Ultra-Low Voltage Drop	
B. Process:	S18	
C. Fabrication Location:	USA	
D. Assembly Location:	Taiwan	Malaysia, Thailand
E. Date of Initial Production:	December 15, 2016	

III. Packaging Information

A. Package Type:	4-bump thin WLP	5-pin SOT23
B. Lead Frame:	N/A	Copper
C. Lead Finish:	N/A	100% matte Tin
D. Bondwire:	N/A (N/A mil dia.)	Au (1 mil dia.)
E. Mold Material:	None	epoxy with silica filler
F. Assembly Diagram:	#05-100399	#05-100457
G. Flammability Rating:	Class UL94-V0	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
I. Single Layer Theta Ja:	N/A°C/W	324.3°C/W
J. Single Layer Theta Jc:	N/A°C/W	82°C/W
K. Multi Layer Theta Ja:	104.41°C/W	255.9°C/W
L. Multi Layer Theta Jc:	N/A°C/W	81°C/W

IV. Die Information

A. Dimensions:	29.9213X29.9213 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OZ34-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX40200ANS+T / MAX40200AUK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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