RELIABILITY REPORT

FOR

MAX396CAI+

PLASTIC ENCAPSULATED DEVICES

June 30, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX396CAI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX396/MAX397 low-voltage, CMOS analog multiplexers (muxes) offer low on-resistance (100 max), which is matched to within 6 between switches and remains flat over the specified signal range (10 max). They also offer low leakage over temperature (input off-leakage current less than 1nA at +85°C) and fast switching speeds (transition time less than 250ns). The MAX396 is a 16-channel device, and the MAX397 is a dual 8-channel device. The MAX396/MAX397 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (5pC max) and guarantee electrostatic-discharge (ESD) protection greater than 2000V per Method 3015.7. These muxes operate with a single +2.7V to +16V supply or with ±2.7V to ±8V dual supplies, while retaining CMOS-logic input compatibility and fast switching. The MAX396/MAX397 are pin compatible with the industry-standard MAX306/MAX307, DG406/DG407, and DG506A/DG507A.

II. Manufacturing Information

A. Description/Function:	Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers
B. Process:	SG5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	28-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0301-0719
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	25°C/W
L. Multi Layer Theta Ja:	67.1°C/W
M. Multi Layer Theta Jc:	25°C/W

IV. Die Information

A. Dimensions:	96 X 156 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.6 \times 10^{-9}$

$\lambda = 4.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AG75 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX396CAI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data