

RELIABILITY REPORT
FOR
MAX3941ETG
PLASTIC ENCAPSULATED DEVICES

October 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3941 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3941 is designed to drive an electro-absorption modulator (EAM) at data rates up to 10.7Gbps. It incorporates the functions of a biasing circuit and a modulation circuit, with integrated control op amps externally programmed by DC voltages.

The integrated bias circuit provides a programmable biasing current up to 50mA. This bias current reflects a bias voltage of up to 1.25V on an external 50 Ω load. The bias and modulation circuits are internally connected on chip, eliminating the need for an external bias inductor.

A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. When a clock signal is available, the integrated data-retiming function can be selected to reject input-signal jitter. The MAX3941 receives differential CML signals (ground referenced) with on-chip line terminations of 50 Ω . The output has a 50 Ω resistor for back termination and is able to deliver a modulation current of 40mA_{p-p} to 120mA_{p-p}, with an edge speed of 23ps (20% to 80% typ). This modulation current reflects an EAM modulation voltage of 1.0V_{p-p} to 3.0V_{p-p}.

The MAX3941 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical EAM characteristics. It is available in a compact 4mm x 4mm, 24-pin thin QFN package and operates over the -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|---|------------------------------|
| Supply Voltage VEE | -6.0V to +0.5V |
| Voltage at MODEN, RTEN, PLRT, MODSET, BIASSET | (VEE - 0.5V) to +0.5V |
| Voltage at DATA+, DATA-, CLK+, and CLK | -1.65V to +0.5V |
| Voltage at OUT | -4V to +0.5V |
| Voltage at PWC+, PWC- | (VEE - 0.5V) to (VEE + 1.7V) |
| Current Into or Out of OUT | 80mA |
| Storage Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +85°C) | |
| 24-Pin Thin QFN | 1354mW |
| Derates above +85°C | |
| 24-Pin Thin QFN | 20.8mW/°C |

II. Manufacturing Information

| | |
|----------------------------------|--|
| A. Description/Function: | 10Gbps EAM Driver with Integrated Bias Network |
| B. Process: | GST4-F60 |
| C. Number of Device Transistors: | 1918 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Korea |
| F. Date of Initial Production: | July, 2003 |

III. Packaging Information

| | |
|---|--------------------------------|
| A. Package Type: | 24-Pin Thin QFN (4 x 4) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-filled epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | Buildsheet # 05-9000-0310 |
| H. Flammability Rating: | Class: UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 99 x 68 mils |
| B. Passivation: | Si ₃ N ₄ (Silicon nitride) |
| C. Interconnect: | Au |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.11 \times 10^{-8} \quad \lambda = 10.11 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7114) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M & RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HT30 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3941ETG

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|--------------------|---------------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 150°C Biased Time = 192 hrs. | DC Parameters & functionality | 48 | 0 |
| Moisture Testing (Note 2) | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} <u>3/</u> | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.

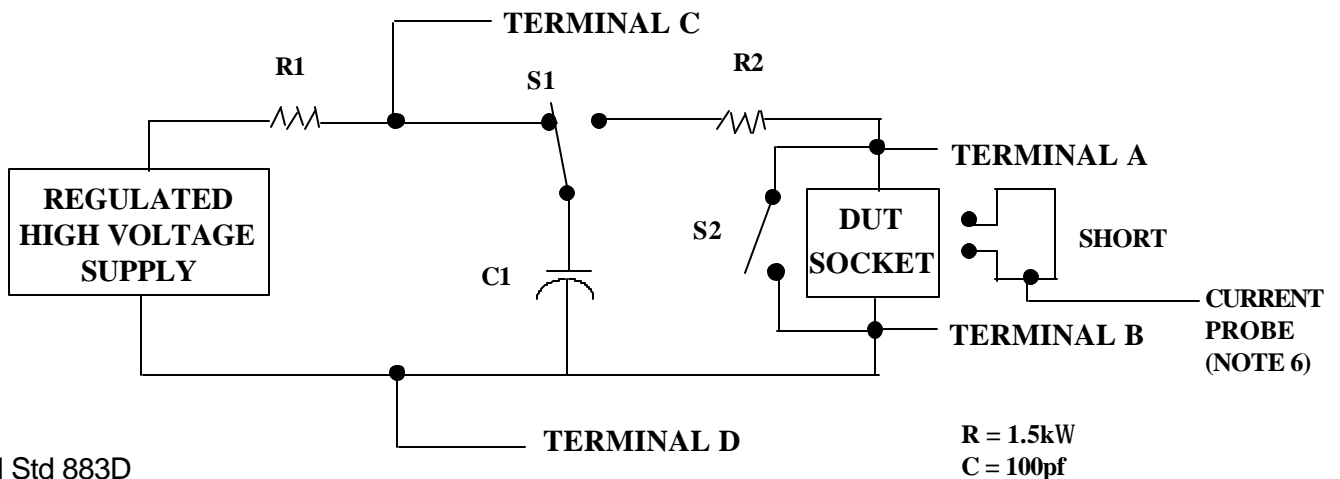
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

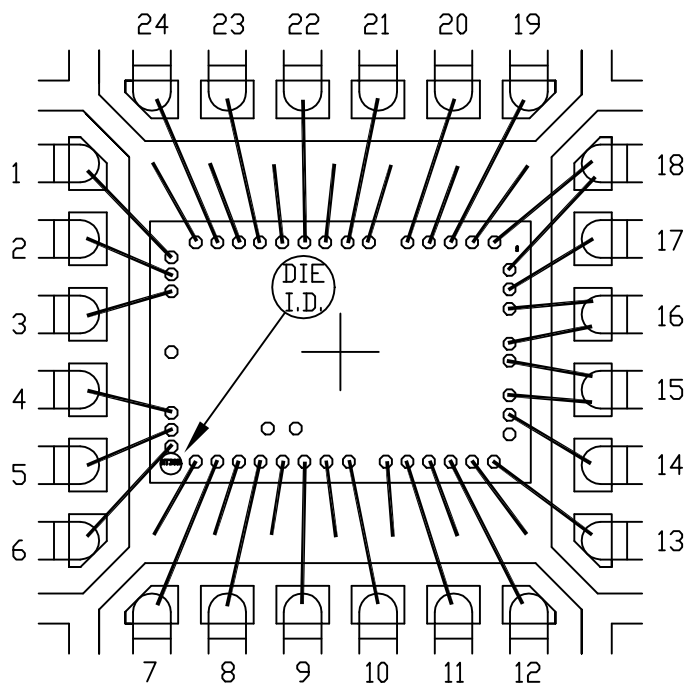
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



4x4x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



| | | | | | |
|---------------------------|----------------|------------|------|---|-----------|
| PKG. CODE: T2444-1 | | SIGNATURES | DATE |  CONFIDENTIAL & PROPRIETARY | |
| CAV./PAD SIZE: 110x110 | PKG. DESIGN | | | BOND DIAGRAM #: 05-9000-0310 | REV: A |

ONCE PER SOCKET

MAX3941 Burn-IN schematic (HT30Z) MAX3942 Burn-In Schematic (HT30Z-1Z)

ONCE PER BOARD

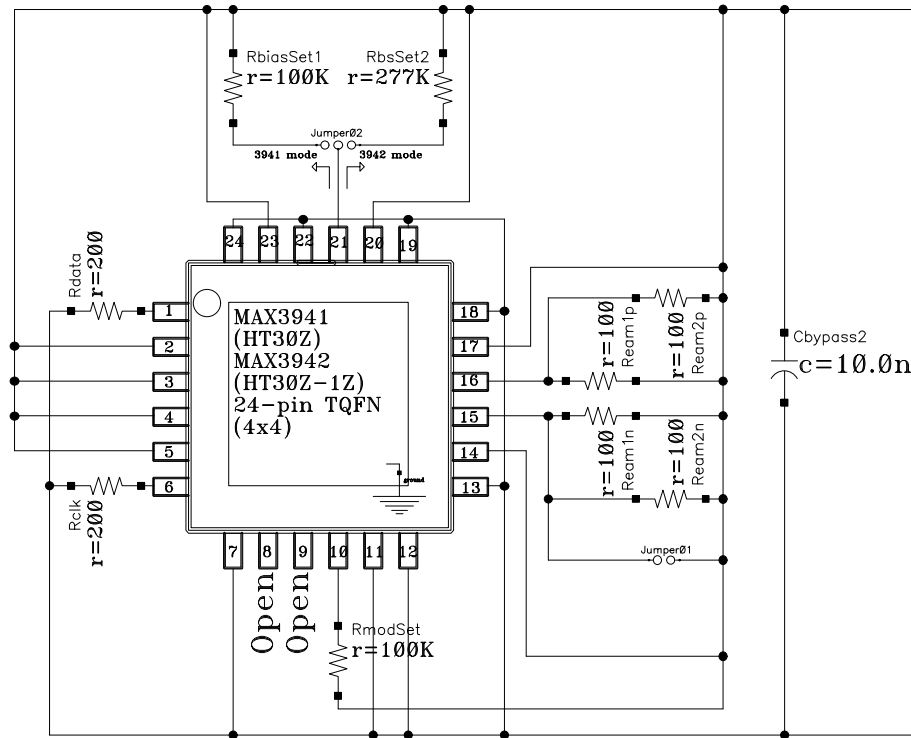
Instructions:

For MAX3941 (HT30Z)

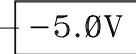
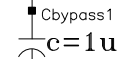
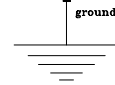
- 1) Short Jumper01
- 2) Short Jumper02 on PIN21-to-RbsSet1 (100K)

For MAX3942 (HT30Z-1Z)

- 1) Open Jumper01
- 2) Short Jumper02 on PIN21-to-RbsSet2 (277K)



Gnd connected to fingers 4-6



-5.5V is preferred if possible
Vee connected to fingers 7/8

Note:

- 1) Vcc is 0V (GROUND)
- 2) Vee is -5.0V, but -5.5V is preferred.
- 3) Vee connected to fingers 7/8
- 4) Gnd connected to fingers 4-6
- 5) Paddle Grounded
- 6) RbsSet2 can be upto 300K
- 5) Package Code T2444-1

HEADER GROUNDED (Yes/No):

PRODUCT: MAX3941 & PACKAGE TYPE: 24-TQFN
 VERSION #: 1 3942 DATE : Oct 25 17:20:56 2002
 ICC (MAX) : 375mA VEE : -5.0V
 VCC : 0 VOLTS (-5.5V preferred)

NOTES: MAX3941 and MAX3942 share the same board but different setting