RELIABILITY REPORT

FOR

MAX3935EGJ

PLASTIC ENCAPSULATED DEVICES

March 15, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3935 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation
.....Attachments

I. Device Description

A. General

The MAX3935 is designed to drive an electro-absorption modulator (EAM) at data rates up to 10.7Gbps. It provides programmable output levels through externally adjustable bias and modulation currents. This EAM driver is fabricated with Maxim's in-house second-generation SiGe process.

The MAX3935 accepts differential ECL or ground-referenced CML clock and data-input signals. Inputs are terminated with on-chip 50Ω resistors. An input-data retiming latch can be used to reject input-pattern-dependent jitter if a clock signal is available.

The driver can modulate EAM devices at amplitudes up to 3.0Vp-p when the device impedance is 50Ω. Typical (20% to 80%) edge speeds are 34ps. The output has an on-chip 75Ω resistor for back termination. The MAX3935 allows for an EAM bias voltage up to 1.2V.

The MAX3935 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical EAM characteristics

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage VEE	-6.0V to +0.5V
VTT	(VEE – 0.5V) to +0.5V
DATA+, DATA- and CLK+, CLK-	(VTT – 1.2V) to the lower of (VTT +1.2V) or +0.5V)
/MODEN, /RTEN, PWC+ and PWC-	(VEE -0.5V) to + 0.5V
MODET and BIASSET Voltage	(VEE – 0.5V) to (VEE + +1.5V)
MOD and BIAS Voltage	(VEE + 1.0V) to +0.5V
Storage Temp.	-55°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = 70°C)	
32-Pin QFN	1860mW
Derates above +70°C	
32-Pin QFN	21.3mW/°C

II. Manufacturing Information

A. Description/Function:	10.7Gbps EAM Driver
B. Process:	GST4
C. Number of Device Transistors:	1535
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	April, 2001

III. Packaging Information

A. Package Type:	**32-Pin QFN**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-7001-0482
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-B:	Level 1

IV. Die Information

A. Dimensions:	120 x 64 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 40 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 12.13 \times 10^{-8}$ $\lambda = 12.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HT11-1 die type has been found to have all pins able to withstand a transient pulse of ± 800V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX3935EGJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	40	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

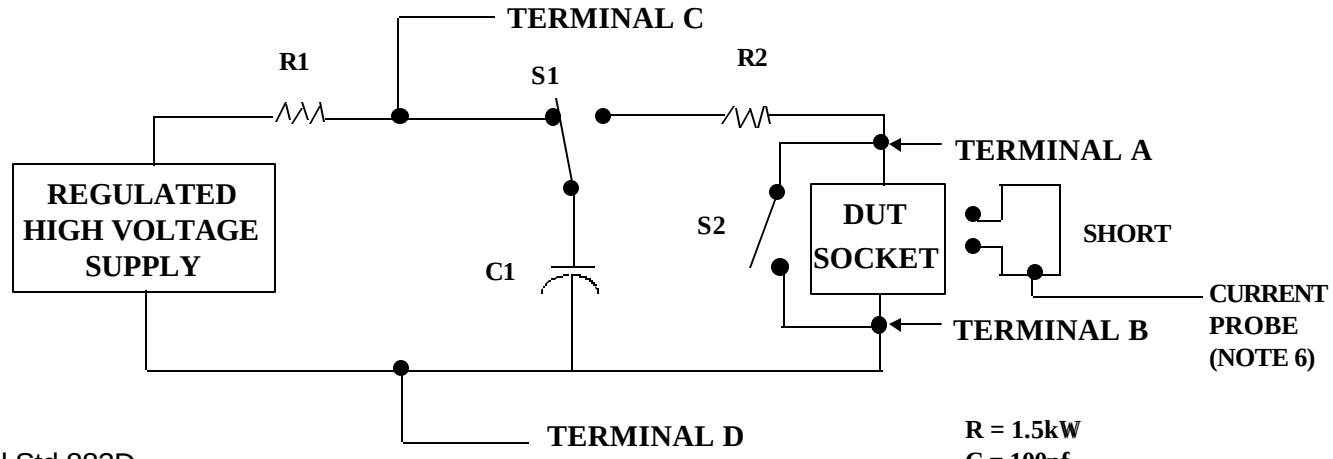
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

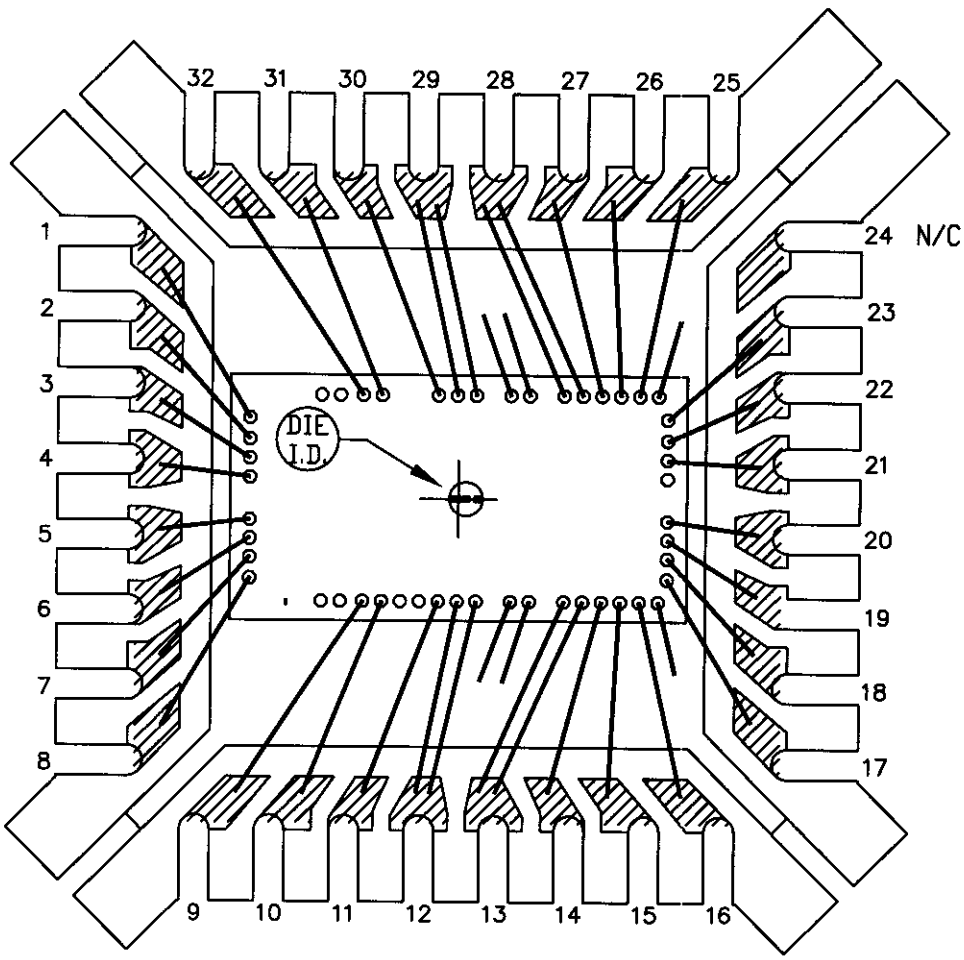
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G3255-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 130x130	PKG. DESIGN			BOND DIAGRAM #: 05-7001-0482 / REV: C